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(81) 指定国(除另有指明, 要求每一种可提供的国家保护): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL,

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(54) Title: CHIP AND INTER-CORE DATA TRANSMISSION METHOD

(54) 发明名称: 一种芯片及核间数据传输方法

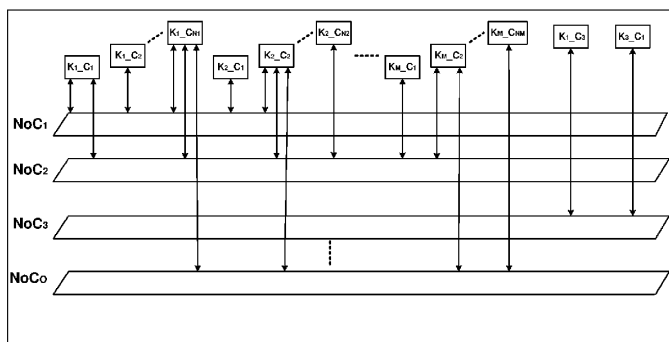


图 2

(57) Abstract: Provided is a chip and an inter-core data transmission method. The chip comprises: a plurality of interconnection structures, wherein each of the interconnection structures is connected to a processing core group, and the processing core group comprises at least two processing cores; data transmission between the processing cores in the processing core group is performed by means of the interconnection structure which is connected to the processing core group; and the plurality of interconnection structures are not directly connected to each other. In the chip, data transmission between cores in the same processing core group is realized by means of the interconnection structure corresponding to the group, and data transmission between cores in different processing core groups can be handled in parallel, such that a total data bandwidth is greatly increased, the efficiency of data transmission between cores is improved, the power consumption is reduced, and the performance of the chip is improved; moreover, since data transmission of different groups can be handled in parallel, the data transmission of different groups will not interfere with each other, thereby preventing the occurrence of a data congestion phenomenon and improving the performance of the chip.

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ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US,
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本国际公布:

— 包括国际检索报告 (条约第21条(3))。

(57) 摘要: 一种芯片及核间数据传输方法。该芯片包括: 多个互联结构, 每个所述互联结构连接一个处理核组, 所述处理核组包括至少两个处理核; 所述处理核组内的各个所述处理核通过与所述处理核组连接的所述互联结构进行数据传输; 其中, 多个所述互联结构之间不直接相连。该芯片中同一处理核组的各个核之间通过与该组对应的互联结构实现数据传输, 不同处理核组的核与核之间的数据传输能够并行处理, 一方面, 大大提高了总的带宽, 提高了核与核之间的数据传输效率, 降低了功耗, 提高了芯片的性能; 另一方面, 由于不同组的数据传输能够并行处理, 不同组的数据传输不会相互干扰, 从而避免发生数据拥塞现象, 提高了芯片的性能。