

A Non-Volatile Memory Device Capable of Initiating Transactions

Background

[0001] This relates generally to non-volatile memories.

[0002] A non-volatile memory is a microelectronic memory that stores data even when power is removed. Examples of non-volatile memories include static random access memories, flash memories, and phase change memories, to mention a few examples.

[0003] Generally, a non-volatile memory is coupled to a memory controller which basically controls all operations of the non-volatile memory. The non-volatile memory then is basically a reservoir of data which is accessed by the memory controller. Transactions between the memory controller and the non-volatile memory are initiated by the memory controller.

Brief Description of the Drawings

[0004] Figure 1 is a schematic depiction of one embodiment of the present invention;

[0005] Figure 2 is a system depiction of one embodiment of the present invention; and

[0006] Figure 3 is a system depiction of one embodiment of the present invention.

Detailed Description

[0007] In accordance with some embodiments of the present invention, instead of using the conventional master/slave relationship between the memory controller and the non-volatile memory, a peer-to-peer relationship may be utilized. In the peer-to-peer relationship, the non-volatile memory may initiate transactions.

[0008] As used herein, a "transaction" is any activity, involving something more than the provision of data or information, outside of the non-volatile memory or any request to an entity outside the non-volatile memory. As used herein, the term

"initiate" means to begin a transaction without input from any other external device. As used herein, a non-volatile memory is a microelectronic storage device that retains information when power is off and that includes an array of rows and columns of addressable memory cells.

[0009] Referring to Figure 1, a non-volatile memory 22 may be a single integrated circuit. The non-volatile memory 22 may, for example, be a flash memory, a static random access memory, or a phase change memory, to mention a few examples. The memory 22 may include an array 32 composed of rows and columns of memory cells which are addressable by column and row addressing circuitry. A control 28 may be a processor-based device or a smart logic device, to mention two examples.

[0010] The control is coupled to an external bus 24 when the memory 22 is in use by an interface 26, in one embodiment. The control 28 may have a storage 30 which is separate from the array 32 in some embodiments. For example, the storage may be a code storage that may be implemented by static random access memory. However, in other embodiments, the control 28 may use memory cells in the array 32. Thus, in some embodiments, the interface, the control, the storage, and the array are all integrated in the same integrated circuit substrate.

[0011] The memory 22 may be provided in one single package and, in some embodiments, may be completely compatible with sockets or receivers traditionally used for mounting packaged non-volatile memory integrated circuits. The size of the packaged integrated circuit memory 22 and its pin configuration may be completely compatible with existing sockets and other devices that receive such devices. In some embodiments, the memory 22 may be used in place of conventional non-volatile memories in the same positions and locations and in the same way they are conventionally used, except that the memory 22 can initiate transactions.

[0012] The memory 22 may initiate transactions under control of the control 28 in one embodiment. The control 28 may issue requests or other transactions, including communications, through an interface 26 with a bus 24. In some embodiments, outgoing communications may be implemented through a separate pin connection on the external package. In other embodiments, a pin used for other purposes may

also be used for such outgoing transactions. In some embodiments, the pin used for outgoing transactions may be bidirectional and may receive responses from the memory controller 20.

[0013] The non-volatile memory 22 that can initiate transactions may have a number of applications. One application is in connection with cellular phones where a small footprint and ability to do more functions may make the memory advantageous in many areas. Thus, in some cases, the non-volatile memory 22 may find particular applicability in connection with mobile devices, but its applicability is not so limited.

[0014] Generally, the memory 22 may initiate requests for information on its own initiative without waiting for polling or other outside stimulus. Likewise, the memory 22, in some embodiments, may also provide information to or through the memory controller upon its own initiative, without waiting for polling or other outside stimulus.

[0015] As an example, when the memory controller 20 accesses the memory 22 over a bus 24, the memory 22 on its own may ask for security information, such as a password or authentication. It may receive the password or authentication back from the memory controller, may compare the password or authentication data to information stored on the memory 22, for example, in the storage 30, and may decide whether or not to allow access to the memory. Thus, such a memory may have particular applications in secure information storage, including the storage of highly confidential data and in the storage of code and other information that hackers would like to compromise.

[0016] Similarly, the memory 22 can request the status information from the memory controller. For example, if the memory 22 knows that the memory controller is powered down, or that the memory controller has information that it will not use for a period of time, this information can be used by the memory 22 to decide to perform internal background or maintenance activities, such as wear leveling. In addition, the memory 22 may obtain information about the memory controller status in order to set the power consumption state of the memory 22.

[0017] Also, the memory 22 may request bus access from the memory controller 20 in order to initiate transactions with the rest of a processor-based system. This allows the memory to actively be involved in activities within the system. In some cases, tasks normally performed by the main or central processing unit of the processor-based system may be off loaded to the control 28. This may free the main or central processor to do other activities. It may also enable transferring activities from the memory controller 20 in some embodiments.

[0018] As still another example, the memory 22 may initiate transactions in order to self-configure itself. For example, the memory 22 may initiate transactions to cause the system to provide information to the memory 22 to facilitate such configuration. It may also obtain preference information from the system in order to configure the memory 22. The memory 22 may configure itself by setting partition sizes, ignoring requests to certain addresses, operating at different speeds or in different read modes, such as burst, page mode, or other modes, offer alternatives, or ask for synchronous speed information so that the memory either speeds up or slows down to either operate more quickly or to save power when operating speed is less important.

[0019] Thus, referring to Figure 2, a processor-based system 10, such as a mobile device, may include the non-volatile memory 14 which is made up of the packaged, single integrated circuit 22. The system 10 may be any mobile device or a non-mobile device. One application for the non-volatile memory device 14 may be in connection with cellular telephones. The non-volatile memory device 14 may interact with a system controller 12. The system controller may be a memory controller, in some embodiments, or may be a controller at any level in a system architecture from a central processing unit down to the memory controller. The system may include other devices 18 and 16 as depicted.

[0020] In some embodiments, the memory device 14 may receive inputs, as indicated by the arrow directed toward the non-volatile memory device 14, as is conventional in slave-type non-volatile memory devices. However, the non-volatile memory device 14 may also initiate transactions, as indicated by the outgoing arrow.

These transactions may include data that is offered by the non-volatile memory without stimulus from the outside of the non-volatile memory device 14. It may also include alerts, as indicated in Figure 2, to indicate non-volatile memory issues, including memory defects, memory capacity, memory speed, security concerns, power consumption state, and wear leveling, to mention a few examples.

[0021] In addition to having a direct access to the system controller 12, as indicated by Figure 2, the non-volatile memory device 14 may have a shared connection to the system controller 12, as indicated in Figure 3. In this embodiment, the communications may include outgoing requests from the non-volatile memory device 14 and responses, indicated by the term "allow," as well as bidirectional data. Thus, the system 20 may allow the non-volatile memory device to directly initiate transactions in some circumstances.

[0022] References throughout this specification to "one embodiment" or "an embodiment" mean that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one implementation encompassed within the present invention. Thus, appearances of the phrase "one embodiment" or "in an embodiment" are not necessarily referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be instituted in other suitable forms other than the particular embodiment illustrated and all such forms may be encompassed within the claims of the present application.

[0023] While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

1. A non-volatile memory comprising:
a memory array; and
a control coupled to said array, said control to initiate a transaction with
a device outside said non-volatile memory.
2. The memory of claim 1 wherein said control and memory array are
integrated on a single integrated circuit.
3. The memory of claim 2 including a storage to store instructions for
execution by said control.
4. The memory of claim 1 wherein said control to initiate a transaction
without first receiving an outside stimulus related to said transaction.
5. The memory of claim 1 including a control to seek security
authorization from a device attempting to access said memory.
6. The memory of claim 1, said control to initiate a transaction including a
request for bus access by said memory.
7. The memory of claim 1, said control to initiate a transaction including a
request for information from said memory controller.
8. The memory of claim 1, said control to request information to enable
said memory to configure itself.
9. The memory of claim 1, said memory adapted to be received in a
conventional non-volatile memory mounting arrangement.

10. The memory of claim 1 wherein said control to initiate a transaction that requests information from a device outside said non-volatile memory.

11. A method comprising:
enabling a non-volatile memory to initiate a transaction with a device outside said non-volatile memory.

12. The method of claim 11 including integrating a control and a memory array for said memory on a single integrated circuit.

13. The method of claim 12 including integrating a storage to store instructions for execution by said control on said integrated circuit.

14. The method of claim 11 including initiating a transaction that involves a request for information from a device outside said non-volatile memory.

15. The method of claim 11 including enabling the memory to seek security authorization from a device attempting to access said memory.