CLAIMS

What is claimed is:

1. A phase change memory (PCM) device comprising:

a bottom electrode;

a bottom heater over the bottom electrode;

a bottom buffer layer over the bottom heater;

a PCM region over the bottom buffer layer;

a top buffer layer over the PCM region;

a top heater over the top buffer layer; and

a top electrode over the top heater;

wherein:

the bottom heater, the bottom buffer layer, the PCM region, the top buffer layer, and the top heater form a PCM pillar,

a layer of isolation layer dielectric (ILD) material is provided on both sides of the PCM pillar,

another layer of ILD material is provided on both sides of the top electrode,

one end of the top electrode is in contact with a portion of a top surface of the layer of ILD material on one side of the PCM pillar, another end of the top electrode is in contact with a portion of a top surface of the layer of ILD material on another side of the PCM pillar;

a via is provided penetrating the layer of ILD material on one side of the PCM pillar, wherein the via extends from directly above the bottom electrode to the upper surface of the layer of ILD material positioned on one side of the top electrode, wherein a same material as the bottom electrode is deposited within the via.

2. The PCM device according to claim 1, wherein the bottom buffer layer comprises a material selected from the group consisting of: C, TiN, TaN, TiC, TaC, TiAlN, TaAlN, TiAlC, TaAlC, HfN, and WN.

3. The PCM device according to claim 1 wherein the bottom heater comprises titanium nitride or tantalum nitride.

4. The PCM device according to claim 1 wherein the PCM region comprises a material selected from the group consisting of: GeTe, Sb_2Te_3, GaSb, AlSb, $Ge_2Sb_2Te_5$, or GST.

5. The PCM device according to claim 1, wherein the PCM region comprises a thickness of less than 100 nm.

6. The PCM device according to claim 1, wherein:

the PCM region comprises a thickness of between 20 and 100 nm; and

the PCM region comprises a material selected from the group consisting of: GeTe, Sb_2Te_3, GaSb, AlSb, $Ge_2Sb_2Te_5$, or GST.

7. A method of fabricating a semiconductor device, the method comprising:

forming a bottom electrode upon a substrate;

forming a bottom heater over the bottom electrode;

forming a bottom buffer layer over the bottom heater;

forming a PCM region over the bottom buffer layer;

forming a top buffer layer over the PCM region;

forming a top heater over the top buffer layer;

etching the bottom heater, the bottom buffer layer, the PCM region, the top buffer layer, and the top heater to form a PCM pillar;

depositing a layer of isolation layer dielectric (ILD) material on both sides of the PCM pillar;

forming a top electrode over the top heater;

depositing another layer of ILD material on both sides of the top electrode, wherein one end of the top electrode is in contact with a portion of a top surface of the layer of ILD material on one side of the PCM pillar, and another end of the top electrode is in contact with a portion of a top surface of the layer of ILD material on another side of the PCM pillar;

etching the layer of ILD material on one side of the PCM pillar to form a via, wherein the via extends from directly above the bottom electrode to a top surface of the layer of ILD material disposed on one side of the top electrode; and

depositing a same material as the bottom electrode in the via.

8. The method according to claim 7, wherein the bottom buffer layer comprises a material selected from the group consisting of: C, TiN, TaN, TiC, TaC, TiAlN, TaAlN, TiAlC, TaAlC, HfN, and WN.

9. The method according to claim 7, wherein the bottom heater comprises tantalum nitride.

10. The method according to claim 7, wherein the PCM region comprises a material selected from the group consisting of: GeTe, Sb_2Te_3, GaSb, AlSb, $Ge_2Sb_2Te_5$, or GST.

11. The method according to claim 7, wherein the PCM region has a thickness of less than 100 nm.