CLAIMS

1. A method of forming large grain copper bitlines for an electronic structure, comprising:

obtaining an MRAM structure including:

a device wafer comprising electronic devices;

a metallized layer over the device wafer and including bottom electrodes therein, the bottom electrodes being electrically connected to the electronic devices; and

vertical pillars having sidewalls above the metallized layer, the vertical pillars each including a magnetic tunnel junction and a top electrode;

forming a copper bitline exhibiting a copper wire size effect over the top electrodes, the copper bitline having a width of forty nanometers or less, an area of three thousand square nanometers or less, and copper grains having relatively small sizes with respect to the width of the copper bitline;

laser annealing the copper bitline, thereby melting the copper bitline; and

recrystallizing the copper bitline during a cool down period following the laser annealing, thereby forming relatively large grains therein and reducing the copper wire size effect of the copper bitline formed over the top electrodes.

2. The method of claim 1, wherein the relatively large grains formed by recrystallizing the copper bitline are vertically aligned with the vertical pillars and include grain boundaries that are mostly over a plurality of spaces between the vertical pillars, and further wherein the vertical pillars have a pitch of sixty nanometers or more along the copper bitline.

3. The method of claim 1, wherein the relatively large grains have an average grain size larger than 0.06 μm after recrystallizing the copper bitline, further wherein recrystallizing the copper bitline includes reducing the copper wire size effect by half or more.

4. The method of claim 3, wherein the copper bitline includes copper at an atomic concentration of at least ninety percent.

5. The method of claim 4, wherein the MRAM structure further includes a dielectric layer between each of the vertical pillars, the relatively large grains including grain boundaries extending mostly over the dielectric layer.

6. The method of claim 5, wherein the laser annealing is conducted at a laser anneal density of from 0.05 to 3 J/cm^2.

7. The method of claim 6, wherein the tunneling magnetoresistance of each magnetic tunnel junction is substantially the same prior to and subsequent to recrystallizing the copper bitline.

8. The method of claim 6, wherein the MRAM structure further includes a metal liner immiscible in liquid copper and extending over the top electrodes and the dielectric layer, further forming the copper bitline directly on the metal liner.

9. The method of claim 1, wherein the vertical pillars have a pitch along the copper bitline at least sixty nanometers.

10. The method of claim 9, wherein laser annealing the copper bitline comprises multiple consecutive copper melt anneals.

11. A method of forming large grain copper bitlines for an electronic structure, comprising:

obtaining an MRAM structure including:

vertical pillars having a pitch of sixty nanometers or more, each of the vertical pillars including a magnetic tunnel junction and a top electrode;

a plurality of spaces respectively between and separating each of the vertical pillars; and

a dielectric layer filling each of the plurality of spaces between the vertical pillars;

forming a copper bitline over the top electrodes and along the pitch of the vertical pillars and extending over the spaces between the vertical pillars, the copper bitline having a width of forty nanometers or less, an area of three thousand square nanometers or less, and copper grains having relatively small sizes with respect to the width of the copper bitline;

laser annealing the copper bitline, thereby melting the copper bitline; and

recrystallizing the copper bitline during a cool down period following the laser annealing, thereby forming relatively large grains therein that are vertically aligned, respectively, with the vertical pillars and having grain boundaries located mostly over the dielectric layer in the spaces between the vertical pillars.

12. The method of claim 11, wherein laser annealing the copper bitline comprises multiple consecutive copper melt anneals and recrystallizing the copper bitline includes multiple cool down periods between the consecutive copper melt anneals.

13. The method of claim 11, wherein the laser annealing is conducted at a laser anneal density of from 0.05 to 3 J/cm^2.

14. The method of claim 11, wherein the MRAM structure further includes a metal liner immiscible in liquid copper and extending over the top electrodes and the dielectric layer, further including forming the copper bitline directly on the metal liner.

15. The method of claim 14, wherein laser annealing the copper bitline includes causing an anneal at or below 1150° C., the metal liner remaining in a solid state during laser annealing.