Fig. 4 is a flowchart of a training sample set acquisition method according to some embodiments of the present disclosure.

Fig. 5 is a flowchart of a method for training a defect detection model based on a training sample set and defect label information according to some embodiments of the present disclosure.

Fig. 6 is a flowchart of a method for acquiring second label information according to some embodiments of the present disclosure.

Fig. 7 is a schematic diagram of a model structure of a defect detection model according to some embodiments of the present disclosure.

Fig. 8 is a schematic diagram of a model structure of another defect detection model according to some embodiments of the present disclosure.

Fig. 9 is a flowchart of a method for screening a defect detection model according to some embodiments of the present disclosure.

Fig. 10 is a flowchart of a defect image classification method according to some embodiments of the present disclosure.

Fig. 11 is a flowchart of a model training and classification process according to some embodiments of the present disclosure.

Fig. 12 is a schematic structural diagram of an apparatus for training a defect detection model according to some embodiments of the present disclosure.

Detailed Description of the Embodiments

In order to enable those skilled in the art to better understand the solutions of the present disclosure, the technical solutions in the embodiments of the present disclosure will be clearly and completely described below in combination with the drawings in the embodiments of the present disclosure. It is apparent that the described embodiments are only part of the embodiments of the present disclosure, not all the embodiments. All other embodiments obtained by those of ordinary skill in the art on the basis of the embodiments in the present disclosure without creative work shall fall within the scope of protection of the present disclosure.

It is to be noted that the terms "first", "second" and the like in the specification, claims and the above drawings of the present disclosure are used for distinguishing similar objects rather than describing a specific sequence or a precedence order. It should be understood that the data used in such a way may be exchanged where appropriate, in order that the embodiments of the present disclosure described here can be implemented in an order other than those illustrated or described herein. In addition, the terms "include" and "have" and any variations thereof are intended to cover non-exclusive inclusions. For example, it is not limited for processes, methods, systems, products or devices containing a series of steps or units to clearly list those steps or units, and other steps or units which are not clearly listed or are inherent to these processes, methods, products or devices may be included instead.

With the development of semiconductor device technology, there are more and more processes for manufacturing semiconductor devices, the main purpose of which is to manufacture circuits and electronic components in a die, such as transistors, capacitors, and logic switches, for example, by performing oxidation and chemical vapor deposition on a die surface, followed by coating, exposure, development, etching, ion