[24] The upper pad 195 and the lower semiconductor pad 255 may be formed of a conductive material, for example, copper or the like, and may be combined and in contact with each other.

[25] The upper insulating layer 190 and the lower semiconductor insulating layer 250 may be formed of an insulating material, for example, silicon oxide, and may be combined and in contact with each other. A material of the upper insulating layer 190 and the lower semiconductor insulating layer 250 may be formed of SiCN or the like, without being limited to silicon oxide.

[26] The semiconductor package 1a may further include a molding layer 310 disposed on the lower structure 100 and covering the semiconductor chip 200.

[27] The semiconductor package 1a may further include a base 10 below the lower structure 100 and a connection structure 50 physically connecting the base 10 and the lower structure 100. The base 10 may be a printed circuit board, an interposer or a semiconductor chip. The connection structure 50 may be a solder ball or a bump.

[28] Next, various examples of the lower structure 100 and the semiconductor chip 200 will be described with reference to FIGs. 2 to 5. FIGs. 2 to 5 are partially enlarged views illustrating various examples of portion “A” in FIG. 1.

[29] In an example, referring to FIGs. 1 and 2, the semiconductor chip 200 described above includes an active side 201f contacting the lower structure 100, and an inactive side 201b opposing the active side 201f. The active side 201f may be referred to as a “lower side”, and the inactive side 201b may be referred to as an “upper side”.

[30] The semiconductor chip 200 may include a semiconductor body 210, a semiconductor internal circuit region 235, the lower semiconductor insulating layer 250 and the lower semiconductor pad 255. The semiconductor internal circuit region 235 may be disposed below the semiconductor body 210, and the lower semiconductor insulating layer

250 and the lower semiconductor pad 255 may be disposed below the semiconductor internal circuit region 235.

[31] The semiconductor body 210 may be a semiconductor substrate, and the semiconductor internal circuit region 235 may be disposed on a lower side 210f of the semiconductor body 210.

[32] The semiconductor internal circuit region 235 may include a semiconductor internal circuit 215 and a semiconductor internal interconnection 240 electrically connecting the semiconductor internal circuit 215 and the lower semiconductor pad 255. The semiconductor internal circuit 215 and the semiconductor internal interconnection 240 may be disposed within a semiconductor internal insulating layer 245.

[33] The semiconductor chip 200 may have the active side 201f and the inactive side 201b opposing each other. The active side 201f of the semiconductor chip 200 may be brought into contact with and coupled to the lower structure 100. In the semiconductor chip 200, the active side 201f may have a width less than that of the inactive side 201b. The semiconductor internal circuit region 235 may have a width less than a width of the inactive side 201b of the semiconductor chip 200.

[34] The lateral side 201s of the semiconductor chip 200 includes the first portion 201s1 and second portion 201s2. The first portion 201s1 may extend from an edge of the inactive side 201b in a direction substantially perpendicular to the inactive side 201b, and the second portion 201s2 may extend from an edge of the active side 201f to the first portion 201s1. The second portion 201s2 includes a vertical portion 201s2a extending from an edge of the active side 201f in a direction substantially perpendicular to the active side 201f, and a curved portion 201s2b extending from the vertical portion 201s2a to the first portion 201s1.

[35] The lower structure 100 illustrated in FIG. 1 may correspond to a lower structure 100a illustrated in FIG. 2. The lower structure 100a may include a lower body 110,

a lower protective insulating layer 165a and a lower connection pad 170a below the lower body 110, a lower internal circuit region 135a on the lower body 110, and the upper insulating layer 190 and the upper pad 195 on the lower internal circuit region 135a. The lower body 110 may be a semiconductor substrate such as a silicon substrate or the like. The lower internal circuit region 135a may be disposed on an active side 110f of the lower body 110, and the lower protective insulating layer 165a and the lower connection pad 170a may be disposed on an inactive side 110b of the lower body 110.

[36] The lower structure 100a may include a penetrating electrode structure 120 penetrating through the lower body 110 to electrically connect the lower connection pad 170a and the upper pad 195. The penetrating electrode structure 120 may include a penetrating electrode 130 formed of a conductive material such as copper or the like, and an insulating spacer 125 surrounding a lateral side of the penetrating electrode 130. The lower internal interconnection 140a may be electrically connected the upper pad 195 and the penetrating electrode 120. The upper pad 195 may be electrically connected to the lower connection pad 170a by the lower internal interconnection 140a and the penetrating electrode 120.

[37] The lower internal circuit region 135a may include a lower internal circuit 115 and a lower internal interconnection 140a electrically connecting the lower internal circuit 115 and the upper pad 195. The lower internal circuit 115 and the lower internal interconnection 140a may be disposed in the lower internal insulating layer 145a.

[38] Thus, the lower structure 100 may be a semiconductor chip 100a including the lower internal circuit region 135a facing the semiconductor chip 200.

[39] In a modified example, referring to FIGs. 1 and 3, the lower structure 100 described above with reference to FIG. 1 may correspond to a lower structure 100b illustrated in FIG. 3. The lower structure 100b may include a lower body 110, a

redistribution region 160b disposed on an inactive side 110b of the lower body 110, a lower internal circuit region 135b disposed on an active side 110f of the lower body 110, and the upper insulating layer 190 and the upper pad 195 disposed on the redistribution region 160b.

[40] The lower internal circuit region 135b may include a lower internal circuit 115, a lower internal interconnection 140b electrically connected to the lower internal circuit 115, and a lower connection pad 150 electrically connected to the lower internal interconnection 140b. The lower internal circuit 115 and the lower internal interconnection 140b may be disposed in the lower internal insulating layer 145b. The lower connection pad 150 may be connected to the connection structure 50 described above.

[41] The redistribution region 160b may include a redistribution pattern 175, a first redistribution insulating layer 167 between the redistribution pattern 175 and the lower body 110, and a second redistribution insulating layer 180 between the first redistribution insulating layer 167 and the upper insulating layer 190.

[42] The lower structure 100b may include a penetrating electrode structure 120 penetrating through the lower body 110 and electrically connecting the lower internal interconnection 140b and the redistribution pattern 175 to each other. Thus, the upper pad 195 and the lower connection pad 150 of the lower structure 100b may be electrically connected to each other through the penetrating electrode structure 120.

[43] Thus, the lower structure 100 may be a semiconductor chip 100b that includes the lower internal circuit region 135b. The lower internal circuit region 135b is formed on the active side 110f of the lower body 110, an inactive side 110b of the lower body 110 faces the semiconductor chip 200, and the lower internal circuit region 135b faces the base 10.

[44] In a modified example, referring to FIGs. 1 and 4, the lower structure 100 described above with reference to FIG. 1 may correspond to a lower structure 100c

illustrated in FIG. 4. The lower structure 100c may include a lower body 110, a redistribution region 160c disposed on an upper inactive side 110b1 of the lower body 110, a lower protective insulating layer 165a and a lower connection pad 107 formed on the lower inactive side 110b2 of the lower body 110, and the upper insulating layer 190 and the upper pad 195 disposed on the redistribution region 160c.

[45] The redistribution region 160c may include the redistribution pattern 175, the first redistribution insulating layer 167, and the second redistribution insulating layer 180, in a manner similar to the redistribution region 160b described with reference to FIG. 3. The lower structure 100c may include a penetrating electrode structure 120 penetrating through the lower body 110 and electrically connecting the redistribution pattern 175 and the lower connection pad 107.

[46] Thus, the lower structure 100c may be an interposer including the redistribution region 160c facing the semiconductor chip 200.

[47] In a modified example, referring to FIGs. 1 and 5, the lateral side 201s of the semiconductor chip 200 may include a modified second portion 201s2', together with the first portion 201s1 described above with reference to FIGs. 1 and 2. In this case, because the remaining components, other than the second portion 201s2' of the lateral side 201s, are described above with reference to FIGs. 1 and 2, a detailed description thereof will be omitted.

[48] The second portion 201s2' of the semiconductor chip 200 may include a vertical portion 201s2a extending from an edge of the active side 201f of the semiconductor chip 200 in a direction substantially perpendicular to the active side 201f, a first curved portion 201s2ba extending from the vertical portion 201s2a, and a second curved portion 201s2bb extending from the first curved portion 201s2ba to the first portion 201s1 and distinguished from the first curved portion 201s2ba.

What is Claimed is:

1. A semiconductor package comprising:

a base; and

a first semiconductor chip provided on the base;

a second semiconductor chip on the first semiconductor chip,

wherein the first semiconductor chip comprises:

a first semiconductor body;

a first lower insulating layer covering a lower surface of the first semiconductor body;

a first semiconductor internal circuit region on an upper surface of the first semiconductor body; and

a first pad and a first upper insulating layer on the first semiconductor internal circuit region,

wherein the second semiconductor chip comprises:

a second semiconductor body;

a second semiconductor internal circuit region below a lower surface of the second semiconductor body; and

a second pad and a second lower insulating layer below the second semiconductor internal circuit region,

wherein the second lower insulating layer is in direct contact with and coupled to the first upper insulating layer,

wherein the second pad is in direct contact with and coupled to the first pad, and

wherein a lateral side of the second semiconductor chip extends between an upper side and a lower side of the second semiconductor chip and comprises a recessed portion.

2. The semiconductor package of claim 1, wherein the lateral side of the second semiconductor chip further comprises a first portion extending from the upper side to the recessed portion in a first direction that is substantially perpendicular to the upper side, and

wherein the recessed portion extends from the lower side to the first portion.

3. The semiconductor package of claim 2, wherein the recessed portion comprises a vertical portion and a curved portion,

wherein the vertical portion extends from the lower side in a second direction that is substantially perpendicular to the lower side, and

wherein the curved portion extends from the vertical portion to the first portion.

4. The semiconductor package of any one of claims 1 to 3, wherein the first semiconductor chip is wider than the second semiconductor chip.

5. The semiconductor package of claim 1, wherein the second semiconductor internal circuit region is narrower than the upper side of the second semiconductor chip.

6. The semiconductor package of any one of claims 1 to 5, wherein the first semiconductor internal circuit region comprises an internal interconnection,

wherein the first semiconductor chip further comprises a penetrating electrode and a lower pad,

wherein the lower pad is below the first lower insulating layer, and

wherein the penetrating electrode is electrically connected to the lower pad and the internal interconnection, and penetrates through the first semiconductor body and the first lower insulating layer.

7. The semiconductor package of claim 6, wherein the first semiconductor body comprises a silicon substrate.

8. The semiconductor package of any one of claims 1 to 7, further comprising a molding layer contacting the first semiconductor chip and the second semiconductor chip, and

wherein the molding layer contacts the lateral side of the second semiconductor chip and a portion of an upper surface of the first upper insulating layer.

9. The semiconductor package of claim 8, further comprising a heat dissipation structure provided on the molding layer and the second semiconductor chip.

10. A semiconductor package comprising:

a lower structure; and

a semiconductor chip provided on the lower structure and having an upper side and a lower side that opposes the upper side,

wherein the lower structure comprises an upper pad and an upper insulating layer,

wherein the semiconductor chip comprises:

a semiconductor body;

a semiconductor internal circuit region below a lower surface of the semiconductor body; and

a lower pad and a lower insulating layer below the semiconductor internal circuit region,

wherein the lower pad is in direct contact with and coupled to the upper pad,

wherein the lower insulating layer is in direct contact with and coupled to the upper insulating layer, and

wherein the lower side of the semiconductor chip is narrower than the upper side of the semiconductor chip.

11. The semiconductor package of claim 10, further comprising a molding layer disposed on a lateral side of the semiconductor chip extending between the upper side and the lower side.

12. The semiconductor package of claim 11, wherein a first portion of the upper insulating layer is in direct contact with the lower insulating layer, and a second portion of the upper insulating layer is in direct contact with the molding layer.

13. The semiconductor package of any one of claims 10 to 12, wherein the lower structure further comprises:

a silicon substrate;

a redistribution pattern electrically connected to the upper pad, and disposed between the upper insulating layer and the silicon substrate; and

a penetrating electrode electrically connected to the redistribution pattern, and penetrates through the silicon substrate.

14. A semiconductor package comprising:

a base; and

a plurality of semiconductor chips provided on the base,

wherein the plurality of semiconductor chips comprises a first semiconductor chip and a second semiconductor chip in direct contact with each other,

wherein the first semiconductor chip has a first upper side and a first lower side that opposes the first upper side,

wherein the second semiconductor chip has a second upper side and a second lower side that opposes the second upper side,

wherein the first semiconductor chip comprises:

a first semiconductor body;

a protection insulating layer on an upper surface of the first semiconductor body;

an upper pad and an upper insulating layer disposed on the protection insulating layer;

a first semiconductor internal circuit region disposed below a lower surface of the first semiconductor body; and

a penetrating electrode penetrates through the first semiconductor body and the protection insulating layer,

wherein the second semiconductor chip comprises:

a second semiconductor body;

a second semiconductor internal circuit region disposed below a lower surface of the second semiconductor body; and

a lower pad and a lower insulating layer disposed below the second semiconductor internal circuit region,

wherein the lower insulating layer and the upper insulating layer are in direct contact with and coupled to each other,

wherein the lower pad and the upper pad are in direct contact with and coupled to each other, and

wherein the second lower side of the second semiconductor chip is narrower than the second upper side of the second semiconductor chip.

15. The semiconductor package of claim 14, wherein the second lower side of the second semiconductor chip is narrower than the first upper side of the first semiconductor chip.

16. The semiconductor package of claim 14 or claim 15, wherein the first lower side of the first semiconductor chip and the second lower side of the second semiconductor chip have a same width, and

wherein the first upper side of the first semiconductor chip and the second upper side of the second semiconductor chip have a same width.