ABSTRACT

There is a 3D semiconductor device comprising a first active region on a substrate and including a lower channel pattern and a lower source/drain pattern connected to the lower channel pattern, a second active region above the first active region and including an upper channel pattern and an upper source/drain pattern connected to the upper channel pattern, at least one gate electrode on the lower and upper channel patterns, a first active contact electrically connected to the lower source/drain pattern, and a second active contact electrically connected to the upper source/drain pattern. A first central line of the lower source/drain pattern and a second central line of the upper source/drain pattern in a vertical direction are offset from each other in a first direction perpendicular to the vertical direction. The first active contact and the second active contact are spaced apart from each other in the first direction.

FIG. 4C