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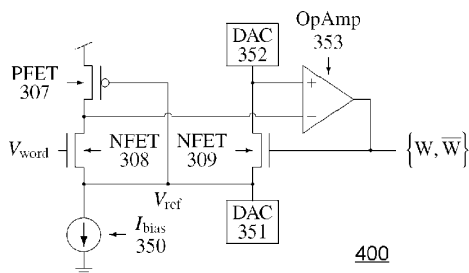
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(54) Title: MULTI-LEVEL DRIVE OF CONTENT ADDRESSABLE MEMORY (CAM) CELLS



(57) Abstract: A content addressable memory (CAM) circuit includes a word line driver that incorporates a digital-to-analog converters (DAC), which enables the CAM circuit to store an n-bit value only with n CAM cells. The CAM circuit includes one or more of CAM cells configured to store bit values, at least one word line driver coupled to word lines of the CAM cells and configured to supply word line output to drive the CAM cells, and at least one bit line driver coupled to bit lines of the CAM cells and configured to supply bit line outputs to drive the CAM cells. The word line driver and the bit line driver include DAC circuits that includes PFETs and NFETs.

FIG. 4