elements do not contact each other but are indirectly joined together via another element or intermediate elements. Finally, the terms "on," "overlying," and "over" may be used in the following description and claims. "On," "overlying," and "over" may be used to indicate that two or more elements are in direct physical contact with each other. However, "over" may also mean that two or more elements are not in direct contact with each other. For example, "over" may mean that one element is above another element but not contact each other and may have another element or elements in between the two elements.

FIG. 1 illustrates an exemplary prior art method 100 of making a wafer level chip scale package. A plurality of semiconductor devices 102 are cut from a wafer. Each semiconductor device 102 has a plurality of protruding bonding pads 104 located on the active surface of the device.

The plurality of semiconductor devices 102 are disposed on the top surface of a retractable film 106. The retractable film 106 is secured by a frame 108. The frame 108 is fixed by a fixture 110 and retractable film 106 is displaced on a work platform 112 and then stretched.

The platform 112 can move up relative to fixture 110. The wafer is cut by a cutter into the plurality of semiconductor devices 102 as shown, which have been encapsulated into semiconductor packages, and then sawn by cutter 118. A shaft 114 moves upward to lift platform 112 relative to fixture 110.

The present invention improves upon the exemplary prior art method 100 of manufacture to render a through-hole via (THV) semiconductor device which is, in some embodiments, stacked together for specific applications and implementations.

FIGs. 2A and 2B illustrate a first embodiment of a

a row of half-cut dummy vias 924 on the left side of die 202, and a row of THVs 902, on the right side of die 202, again disposed in organic material 602.

FIG. 26 illustrates a ninth exemplary embodiment of a THV stackable semiconductor device 928, depicting two stacked dies 202 and 203 utilizing dummy via holes 902 as shown in FIGs. 24 and 25 to connect a top die 203 with a wire-bonding process. A series of bond pads 205 is disposed on an active surface of die 203. Wire-bonds 207 connect bond pads 20~~4~~5 to vias 902. A dielectric, insulating or bonding material 209 is disposed between die 202 and die 203 to provide structural support for device/package 928.

Semiconductor devices, such as device 200 incorporating a series of THVs 226 or 902 can provide a variety of functionality and flexibility in various applications. Use of organic material 210 allows placement of vias 226 outside die 202, which allows for additional circuitry within die 202 and enhancing the functionality of device 200. In addition, by using organic material 210 instead of wafer 300 material, the respective yield per wafer is increased. The organic material can be configured to be as thick as needed to accommodate a variety of vias 226 in any number of applications.

Device 200 can be incorporated into a variety of package-on-package(PoP) configurations, which make use of THV 226. Such a device can include a semiconductor die having an integrated THV 226. Such a semiconductor die can be referred to as a THV die. Current package-in-package (PiP) packaging techniques make use of wire and/or bump interconnections to provide electrical signals between dies, interposers, and packages. There is growing demand to provide more robust, efficient and space saving interconnections. The use of THV

structures like 226, and

or integrated circuit package 304 is disposed over THV die 202 using bumps 306.

FIG. 42 illustrates a package 308 which again incorporates ~~an inverted~~ a bottom package 286. A solder paste 310 is coupled to the bottom surface of via 226. A passive device 312, such as an inductor, filter, capacitor, resistor, or similar passive device 312 is coupled to solder paste 310 to provide additional functionality to package 308. In the depicted embodiment, THV die 202 overhangs package 286, allowing the room for passive devices 312. An encapsulant 211 covers portions of all of the components of package 308 as shown to provide structural support. A bond pad 314 couples THV die 202 to substrate 230 at location 294.

In an additional embodiment shown in FIG. 43, PiP 316 again includes THV die 202 with attached passive devices 312 using a solder paste material 310, where devices 312 are attached to the top surface of vias 226. A~~n inverted~~ bottom package 318 can again include such configurations as QFN, SON, QFP, LGA, BGA, flip chip bare dies, and WLP ~~configurations 318~~. A bond pad 314 couples THV die 202 through passive device 312 to the substrate using wires 20~~9~~7. Again, an encapsulant 211 is then provided for structural support of package 316.

As the various PiP embodiments illustrate, a variety of innovative, robust, flexible, and efficient PiP configurations can be realized using THV 226 of THV die 202.

While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

What is claimed:

1. A semiconductor device, comprising:

a first semiconductor die;

an insulating material disposed around a peripheral region of the first semiconductor die including a first surface of the insulating material coplanar with a first surface of the first semiconductor die;

a conductive via formed through the insulating material with a side surface of the conductive via coplanar with a side surface of the insulating material;

a ~~redistribution layer including a first~~ bond pad formed ~~over a~~on the first surface of the first semiconductor die;

a conductive trace formed between the bond pad and the conductive via; and

a second semiconductor die disposed over the first surface of the first semiconductor die ~~and redistribution layer~~.

~~2. The semiconductor device of claim 1, further including:~~

~~a second bond pad formed over the surface of the first semiconductor die; and~~

~~a conductive trace formed over the surface of the first semiconductor die between the conductive via and the second bond pad.~~

~~3~~2. The semiconductor device of claim 1, further including an encapsulant deposited over the ~~first and~~ second semiconductor die and around the insulating material, wherein the encapsulant contacts the side surface of the conductive via.

~~4~~3. The semiconductor device of claim 1, further including a third semiconductor die disposed over the first semiconductor die or the second semiconductor die.

~~5~~4. The semiconductor device of claim 1, further including a bond wire ~~electrically coupled~~ mechanically bonded to a first surface of the conductive via coplanar with the first surface of ~~to~~ the first semiconductor die

~~or the second semiconductor die~~ and the first surface of the insulating material.

~~6~~5. The semiconductor device of claim 1, further including a substrate, wherein the first semiconductor die is disposed over the substrate.

~~7~~6. A semiconductor device, comprising:

a first semiconductor die;

an insulating material disposed around a peripheral region of the first semiconductor die including a surface of the insulating material coplanar with a surface of the first semiconductor die;

a conductive via formed through the insulating material with a top surface, a side surface, and a bottom surface of the conductive via exposed from the insulating material;

a ~~first~~ bond pad formed ~~over~~on ~~a~~the surface of the first semiconductor die; and

~~a conductive trace formed over the surface of the first semiconductor die between the conductive via and the first bond pad; and~~

~~a redistribution layer including a second bond pad formed over the surface of the first semiconductor die~~

a conductive trace coupled between the conductive via and the bond pad.

~~8~~7. The semiconductor device of claim ~~7~~6, further including:

a second semiconductor die disposed over the first semiconductor die; and

an encapsulant deposited over the ~~first and~~ second semiconductor die and contacting the insulating material.

~~9~~8. The semiconductor device of claim ~~8~~7, further including a third semiconductor die disposed over the first semiconductor die or the second semiconductor die.

~~10~~9. The semiconductor device of claim ~~9~~8, wherein the third semiconductor die overhangs the second semiconductor die.

1~~1~~0. The semiconductor device of claim ~~8~~7, wherein the second semiconductor die overhangs the first semiconductor die.

1~~2~~1. The semiconductor device of claim ~~8~~7, further including a bond wire electrically coupled to the first semiconductor die or the second semiconductor die.

1~~3~~2. The semiconductor device of claim ~~7~~6, further including an integrated passive device disposed over the first semiconductor die.

1~~4~~3. A semiconductor device, comprising:

a first semiconductor die;

an insulating material disposed around a peripheral region of the first semiconductor die;

a half-cut conductive via formed through the insulating material; and

a ~~redistribution~~ conductive layer formed ~~over~~ on a surface of the first semiconductor die and a surface of the insulating material and coupled to the conductive via.

1~~5~~4. The semiconductor device of claim 1~~4~~3, further including~~:~~

a bond pad formed over the surface of the first semiconductor die~~; and~~

~~a conductive trace formed over the surface of the first semiconductor die between the conductive via and the bond pad~~ and coupled to the conductive via through the conductive layer.

1~~6~~5. The semiconductor device of claim 1~~4~~3, further including an encapsulant deposited over the first semiconductor die and contacting the insulating material.

176. The semiconductor device of claim 143, further including a second semiconductor die disposed over the first semiconductor die.

187. The semiconductor device of claim 176, further including a third semiconductor die disposed over the first semiconductor die or the second semiconductor die.

198. The semiconductor device of claim 176, further including a bond wire electrically coupled to the first semiconductor die or the second semiconductor die.

2019. A semiconductor device, comprising:

a first semiconductor die;

an insulating material disposed around a peripheral region of the first semiconductor die;

a conductive via formed through the insulating material with a side surface of the conductive via exposed at a side surface of the insulating material; and

a conductive trace formed overon a surface of the first semiconductor die and ~~electrically coupled~~ extending to the conductive via.

~~21. The semiconductor device of claim 20, further including a redistribution layer formed over the surface of the first semiconductor die.~~

2220. The semiconductor device of claim 2019, further including an encapsulant deposited over the first semiconductor die.

2~~3~~1. The semiconductor device of claim ~~20~~19, further including a second semiconductor die disposed over the first semiconductor

die.

242. The semiconductor device of claim 231, further including a third semiconductor die disposed over the first semiconductor die or the second semiconductor die.

253. The semiconductor device of claim 231, further including a bond wire electrically connected to the first semiconductor die or the second semiconductor die.