ABSTRACT

A digital signal processor comprises an arithmetic device 12 wherein a reservation processing register 26, to which setting to which from the arithmetic device 11 is possible and which has a construction for storing an address and an execution mode as a task list 18, and a clear circuit 27 for clearing the execution mode when the address in the reservation processing register 26 is copied to a program counter 21, are newly added.

Thereby, in the digital signal processor comprising two arithmetic devices, it is possible to remove the processing waiting time as well as to change the processing order at respective arithmetic devices.