

APPARATUS AND METHOD FOR CONTROLLING
PWM-CONTROLLED VOLTAGE TYPE INVERTER

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This invention relates to a control system for controlling a PWM-controlled voltage source inverter, and more particularly to an apparatus and method suitable for the PWM control of a voltage source inverter according to a software program using a microcomputer.

As prior art apparatus designated for the PWM control of voltage source inverters, both of those based on a method using an analog circuit and those based on a method using a digital circuit are already known.

A prior art PWM control apparatus based on the former method is disclosed in, for example, a book entitled "New Drive Electronics" written by Naohiko Kaniyama and published by Denki Shoin Publishing Co. in Japan in July, 1986. According to the method described at page 92 of this publication, a voltage command signal (a modulation wave signal) representing the error between a current command signal and an output current of a voltage source inverter is compared in an analog circuit with a given triangular wave signal which is a carrier wave signal, so as to generate a desired pulse pattern used for controlling the PWM-controlled voltage source inverter. In a modification of the former method, the modulation wave signal and the carrier wave signal are compared in a digital fashion. Herein, such a modification is

1 classified to belong to the former method.

A prior art PWM control apparatus for controlling a voltage source inverter according to the latter method using a digital circuit is disclosed in, for example, Japanese Patent Publication No. 55-49509 filed as
5 a patent application by Mitsubishi Electric Co., Ltd. In Japan on December 28, 1973 and published on December 12, 1980. The cited publication proposes a method which attempts to generate an improved rectangular output from
10 the voltage source inverter by alternately applying on-off control to two phase and generally increasing and decreasing the pulse width of the rectangular wave output.

On the other hand, a method for controlling a current source inverter instead of a voltage source
15 inverter is disclosed in JP-A-62-163577 filed as a patent application by Hitachi, Ltd. on January 11, 1986 and laid open on July 20, 1987. The disclosure of the cited publication proposes to generate a sine wave output from a PWM-controlled current source inverter by converting
20 instantaneous values of a sine wave into corresponding pulse widths. Further, U.S. Patent Application Serial No. 2283, which was filed on January 12, 1987 and whose assigners include some of the inventors of the present application, discloses a method for controlling a current
25 source inverter by a microcomputer.

In the related art described above, any consideration is not especially given to application of the PWM control apparatus for the control of the voltage

1 source inverter according to a software program, and
various problems such as a capability of generation of an
output waveform sufficiently close to a sinusoidal
waveform and a capability of reduction of the size of the
5 PWM control apparatus remain still to be solved.

More specifically, in the case of the PWM
control apparatus based on the method using the analog
circuit, a plurality of comparators each including an
operational amplifier are essentially required, and this
10 requirement leads to problems such as a lot of time and
labor consumed for adjustment of the comparators and an
inevitable increase in the circuit scale. Also, in the
case of the PWM control apparatus based on the method
using the digital circuit, generation of an ideal sine
15 wave output is difficult because the two phases only are
on-off controlled. Further, because the control circuit
is composed of discrete circuit parts, there is yet
considerable room for improvement from the viewpoint of
simplification of the circuit scale.

20 On the other hand, although the methods
disclosed in JP-A-62-163577 and U.S. Patent Application
Serial No. 2283 cited above are satisfactory in that the
PWM signal has a pulse pattern close to the waveform of a
sine wave, and that the structure of the control circuit
25 is simplified, the applicable subject of those methods is
limited to the current source inverter, and the methods
cannot be directly applied to the voltage source inverter.

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It is an object of the present invention to provide an apparatus and method capable of substantially completely controlling a PWM-controlled voltage source inverter according to a software program while satisfying the requirements that the inverter generates a PWM output pattern sufficiently close to a sine wave and the number of discrete circuit parts used in the control circuit can be greatly decreased.

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The control apparatus of the present invention which attains the above object produces a control signal (an on/off signal) for controlling switching elements constituting the inverter according to a control sequence as described below. That is, when a control command value of an inverter output is determined, a control mode corresponding to the control command value is selected from among a plurality of control modes previously contained in a control table, so that the switching elements to which the control signal is applied and the order of controlling the switching elements are determined. Also, on the basis of the control command value, the difference between a modulation signal and a predetermined reference value is computed for each phase to determine the timing of controlling the switching elements. In this case, the unit control period of each control mode is divided into halves, and the timing of controlling the switching elements is determined in the individual halves of the with control period. Then, the

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1 selected control mode is combined with the determined
timing of controlling the switching elements to produce
the control signal.

In the drawings:

5 Fig. 1 is a block diagram showing the structure
of a preferred embodiment of the apparatus for controlling
a PWM-controlled voltage source inverter according to the
present invention.

Figs. 2, 3 and 4 are flow charts for illust-
10 rating the operation of the control apparatus shown in
Fig. 1.

Figs. 5, 6, 7, 8, 9 and 10 are timing charts for
illustrating the operation of the control apparatus shown
in Fig. 1.

15 Figs. 11A and 11B show how PWM pulses are
produced.

Figs. 12 and 13 are flow charts for illustrating
the operation of the control apparatus shown in Fig. 1.

Fig. 14 shows a table containing various pulse
20 patterns in various modes of controlling the switching
elements shown in Fig. 1.

Fig. 15 shows an example of waveforms of the PWM
pulses.

25 Inventors including some of the inventors of the
present application made a proposal in which the apparatus

- 1 used for controlling the PWM-controlled current source
inverter disclosed in JP-A-62-163577 cited already was
applied to an apparatus for controlling a PWM-controlled
voltage source inverter. A patent application disclosing
5 the above proposal was filed as Japanese Patent Appli-
cation No. 62-171026 on July 10, 1987, but has not been
laid open up to now. Also, corresponding patent
applications have not yet been filed in foreign
countries. This earlier application filed in Japan
10 proposes a method comprising the steps of detecting the
difference between the peak value of a modulation wave
signal of each phase and a predetermined reference value
in response to the application of a phase control command,
determining the above value for each phase in a unit
15 control period (the value corresponding to the reciprocal
of the switching frequency), and repeating the above steps
to produce a pulse pattern used for controlling the
switching elements of the voltage source inverter. In the
proposed method, a software program is used to execute the
20 control of the voltage source inverter. However, because
the on/off frequency of the output voltage of the inverter
cannot be made higher than the on/off frequency (the
switching frequency) of the switching elements, it is
difficult to effectively decrease the noise generated from
25 a motor coupled to the inverter.

In the control apparatus embodying the present
invention, the noise generated from the motor can be
effectively decreased by controlling ON/OFF operation of

1 the inverter output voltage in higher frequency than the
switching frequency of the switching elements forming the
inverter. Further details of such embodiment will be
explained below.

5 Fig. 1 is a block diagram showing the structure
of a preferred embodiment of the control apparatus
according to the present invention. Referring to Fig. 1,
the control apparatus includes a d.c. power source 1, an
input terminal 2 for a frequency command signal ω_1^* , an
10 input terminal 3 for a phase command signal θ^* , and an
input terminal 4 for a modulation factor command signal
 γ^* . A main switching circuit 5 of a voltage source inverter
includes a plurality of or six transistors 51 to 56 acting
as semiconductor switching elements. (In Fig. 1, reverse
15 conducting diodes are not shown). The voltage source
inverter is connected through a noise-preventive a.c.
reactor 6 to an induction motor 7 which is a load of the
inverter. The control apparatus further includes a
control-purpose one-chip microcomputer 10 connected to the
20 transistors 51 to 56 of the inverter by PWM control pulse
signal lines 8.

The microcomputer 10 includes an input port 101
connected to the input terminals 2, 3 and 4 for receiving
the control command signals described above, an internal
25 bus 102, a ROM 103 storing various control programs, a
pulse width data table, etc., a RAM 104 used as a
temporary storage and a register, a microprocessor (ALU)
executing arithmetic and logical operations, a mode

1 setting register 107 setting or selecting a control mode
(information concerning the transistors to be controlled
and the order of controlling the transistors) required for
supplying a predetermined pulse pattern to an output port
5 106, a timing setting register 108 setting the timing of
enabling the selected control mode, a hold register 109
holding the combination of the data of the selected
control mode and the data of the control-mode enabling
timing registered in the respective registers 107 and 108,
10 an associative memory 110 including a plurality of memory
units for sequentially storing the data transferred from
the hold register 109 each time the data of the control
mode and the data of the control mode enabling timing are
set, a timer 111 continuously generating an output
15 representing the real time, a comparator 112 comparing the
control timing data stored in the associative memory 110
with the real time output of the timer 111 and generating
a coincidence signal when coincidence is reached there-
between, and an execution controller 113 operating in
20 response to the application of the coincidence signal from
the comparator 112 to read out the combination of the
control mode data and the coinciding control timing data
from the associative memory 110 when the control timing
data stored in one of the memory units of the associative
25 memory 110 does not coincide with the real time data
supplied from the timer 111, the comparator 112 compares
the control timing data stored in the next memory unit of
the associative memory 110 with the real time data

1 supplied from the timer 111. Therefore, only when the
desired control timing coincides with the real time, the
execution controller 113 can decide the control signal to
be applied to control the transistors specified by the
5 control mode data. In response to the application of the
coincidence signal from the comparator 112, the execution
controller 113 receives and checks the control mode data
supplied from the associative memory 110 and decides the
rise time and fall times of pulses of the control signal.
10 Then, the execution controller 113 decides a pin of the
output port 106 to which the control signal is to be
applied among a total of six pins and sends out the
control signal to the main switching circuit 5 through the
selected pin of the output port 106.

15 Fig. 2 is an outline of a flow chart of a pulse
pattern determining program executed for determining the
pulse pattern of the control signal applied to the main
switching circuit 5 through the output port 106 of the
microcomputer 10. In a first step F1100, the frequency
20 command signal ω_1^* and the phase command signal θ^* applied
to the input port 101 of the microcomputer 10 are read.
It is apparent that this reading step F1100 is unnecessary
when the values of ω_1^* and θ^* are computed in the interior
of the microcomputer 10. Then, in a step F1200, the
25 frequency command ω_1^* is integrated at a time interval of
a predetermined period of time Δt_1 , and the phase command
 θ^* is added to the result of integration to compute the
composite phase θ_T (control target phase). Then, in a

1 step F1250, whether or not the value of this target phase θ_T is included within the range of 0° to 360° is checked. When the result of checking proves that the value of the target phase θ_T is not included within the range of 0° to
5 360° , the target phase θ_T is converted into a value which is included within the range of 0° to 360° . Fig. 3 shows details of a flow chart of such processing. First, decision is made in a step F1251 as to whether or not the value of the target phase θ_T is equal to or larger than
10 360° . When the result of decision in the step F1251 is "YES", the target phase θ_T is converted into $(\theta_T - 360^\circ)$ in a step F1252. On the other hand, when the result of decision in the step F1251 is "NO", decision is further made in a step F1253 as to whether the value of θ_T is
15 smaller than 0° . When the result of decision in the step F1253 is "YES". θ_T is converted in a step F1254 into $(\theta_T + 360^\circ)$, and the processing comes to an end. On the other hand, when the result of decision in the step F1253 is "NO", conversion of θ_T is unnecessary, and the
20 processing comes to the end.

In the present invention, six control modes are provided by dividing the electrical angle (the phase) of 360° into six ranges each having an angular range of 60° . In a step F1300 shown in Fig. 2, the most suitable control
25 mode corresponding to the target phase θ_T computed in the step F1200 is decided. That is, the most suitable pulse pattern of the control signal to be applied to the transistors 51 to 56 is decided. The control modes

1 corresponding to the control phases each having the
angular range of 60° are previously determined. For
example, the control modes corresponding to the individual
control phase ranges are stored in the ROM 103 in the form
5 of a table as shown in Fig. 14.

The manner of decision of the pulse pattern in
the step F1300 will be described in further detail with
reference to Fig. 4.

The manner of inverter control in the illust-
10 rated embodiment of the present invention is such that the
pulse pattern is changed every electrical angle range of
 60° , and one round of the six control modes covering the
total electrical angle of 360° is repeated. Thus, one of
the six control modes M1 to M6 each covering the range of
15 60° is selected according to the value of the target phase
 θ_T computed in the step F1200. The flow chart of Fig. 4
shows the manner of selection of the most suitable control
mode.

Thus, when the most suitable control mode
20 corresponding to the value of the target phase θ_T is
selected, the transistors to be on-off controlled and the
order of on-off control are decided.

The practical operation in the individual
control modes M1 to M6 will now be described.

25 In the illustrated embodiment of the present
invention, each control mode is divided into a former half
and a latter half, that is, a step 1 and a step 2, so that
the transistors 51 to 56 are on-off controlled in these

1 steps. By dividing each control mode into the steps 1 and
2 and controlling the transistors 51 to 56 in these steps,
the inverter output voltage (the voltage applied to the
motor) can be controlled at a frequency two times as high
5 as the on/off frequency (the switching frequency) of the
transistors.

Fig. 5 shows the operation in the control mode
M1, that is, the operation when the value of the target
phase θ_T is included within the electrical angle range
10 of 0° to 60° . Fig. 5 shows that the levels of the pulses
applied to the transistors 51, 52 and 53 change after
respective periods of time (control timing) t_1 , t_2 and
 t_3 from time $t = t_0$ in the step 1, and those of the
pulses applied to the transistors 54, 55 and 56 change
15 after respective periods of time (control timing) t_4 ,
 t_5 and t_6 from time $t = \Delta t_1 + t_0$ in the step 2. The
manner of computation of these periods of times t_1 , t_2 , t_3 ,
 t_4 , t_5 and t_6 will be described later. Suppose now that
these periods of time t_1 to t_6 are previously determined
20 as shown. In such a case, the transistors 54, 55 and 56
disposed on the negative arm are initially in their on
state at time $t = t_0$ in the step 1 of the control mode
M1. All of the remaining transistors 51, 52 and 53
disposed on the positive arm are initially in their off
25 state at time $t = t_0$. After the period of time t_3 ,
the transistor 56 on the negative arm is turned off, and
the transistor 53 on the positive arm is turned on.
Similarly, after the period of time t_1 , the transistor

1 54 on the negative arm is turned off, and the transistor
51 on the positive arm is turned on. Also, after the
period of time t_2 , the transistor 55 on the negative arm
is turned off, and the transistor 52 on the positive arm
5 is turned on. In this manner, the transistors 51 to 56
are turned on and off in the order described above.

Then, the transistors 51 and 54 are turned off
and on respectively after the period of time t_4 from
time $t = \Delta t_1 + t_0$, the transistors 52 and 55 are turned
10 off and on respectively after the period of time t_5 , and
the transistors 53 and 56 are turned off and on respec-
tively after the period of time t_6 . The pulse pattern in
the control mode M1 is determined in the manner described
above so that the transistors 51 to 56 are selectively
15 turned on and off. However, the values of the periods of
time t_1 , t_2 and t_3 change depending on the value of the
target phase θ_T . In Fig. 5, the value of the target
phase θ_T is supposed to be very close to 0° , and the
transistors 53, 54 and 55 are turned off in the illust-
20 rated order. However, the order of turning off these
transistors may change, because, as will be seen in Fig.
11A, the positive level of the modulation wave signal of
one phase is reversed from that of the modulation wave
signal of another phase at the boundary where the
25 electrical angle is 30° .

Pulse patterns corresponding to the control
modes M2 to M6 are determined as shown in Figs. 6 to 10
respectively. These control modes M2 to M6 are generally

1 similar to the control mode M1 except that the order of
turning on and off the transistors 51 to 56 is different
from that shown in Fig. 5, and description of the details
of these control modes will be unnecessary.

5 Referring to Fig. 2 again, the periods of time
 t_1 to t_3 and t_4 to t_6 scheduled for changing the pulse
pattern at the interrupt time interval of Δt_1 on the basis
of the value of the target phase θ_T are detected in a
step F1400, by reference to the table stored in the ROM
10 103.

The manner of processing in this step F1400 will
be described with reference to Figs. 11A and 11B.

The modulation wave signal corresponding to each
of the 120° different three phases of the a.c. output of
15 the inverter is expressed as $\sin \theta$, $\sin (\theta - \frac{2}{3} \pi)$ and
 $\sin (\theta - \frac{4}{3} \pi)$. In the illustrated embodiment of the
present invention, two kinds of predetermined reference
values are previously set. That is, a first reference
value X having a level higher than the level of the
20 positive peak value of the modulation signal of each phase
and a second reference value having a level lower than the
level of the negative peak value of the modulation wave
signal of each phase are previously set, and the periods
of time t_1 to t_3 and t_4 to t_6 are computed on the basis of
25 these reference values. The first reference value X, the
second reference value Y and the data of the modulation
wave signal of each phase are stored in the ROM 103, and
the ALU 105 executes the computation of the control

1 timings t_1 to t_6 .

First, when the target phase θ_T is given as shown in Fig. 11A, the differences between the first reference value X and the instantaneous value of the modulation wave signal of each phase at the given target phase θ_T are computed to detect the respective periods of time t_1 , t_2 and t_3 .

Then, when the next target phase $\theta_T + \Delta\theta$ is given as shown in Fig. 11B, the differences between the second reference value Y and the instantaneous value of the modulation wave signal of each phase at the given target phase $\theta_T + \Delta\theta$ are computed to detect the respective periods of time t_4 , t_5 and t_6 .

Thus, the control timing t_1 to t_6 in the control modes shown in Figs. 5 to 10 are given so that the pulse pattern in each step of each control mode can be determined.

When adjustment of the modulation factor γ^* is additionally required, further processing may be made in which the computed periods of time t_1 to t_6 are multiplied by the adjusted modulation factor γ^* .

The target phase $\theta_T + \Delta\theta$ shown in Fig. 11B means the phase detected at the time (the second instant) where the predetermined constant period of time Δt_1 has elapsed from the time (the first instant) where the target phase θ_T shown in Fig. 11A was given. The value $\Delta\theta$ in the target phase $\theta_T + \Delta\theta$ includes an integrated component of the frequency command ω_1^* and a

1 changed component of the phase command θ^* . Also, the
predetermined constant period of time Δt_1 described
above means the time interval of computing the pulse
width. The value of $\Delta\theta$ can be approximated as $\Delta\theta = 0$ when
5 the time interval Δt_1 is very short. Therefore, in the
case of computation of the differences between the second
reference value Y and the instantaneous values of the
modulation wave signal of each phase, the value of the
composite phase θ_T used when computing the differences
10 between the first reference value X and the instantaneous
values of the modulation wave signal of each phase can be
directly used without giving rise to any substantial
problem. In such a case, the pulse pattern in each of the
control modes shown in Figs. 5 to 10 is symmetrical on
15 both sides of $t = \Delta t_1$ to t_0 .

The manner of computation of the periods of time
 t_1 to t_6 in the control mode M1, in which the composite
phase θ_T is included within the range of 0° to 60° and
which is shown in Fig. 5 has been described with reference
20 to Figs. 11A and 11B. The same applies to the remaining
control modes M2 to M6, and any detailed description will
be unnecessary.

The processing described above determines the
two items, that is, the data of the control mode and the
25 data of the control timing to be registered in the two
registers 107 and 108 respectively.

Fig. 12 is a flow chart of a program F2000 for
storing the data of the two items described above in the

1 associative memory 110 provided for controlling the output
port 106 of the microcomputer 10.

First, decision is made in a step 2100 as to
whether or not all the control modes and control timings
5 required for controlling the six transistors 51 to 56 have
been completely stored in the associative memory 110.
When the result of decision in the step F2100 is "NO", the
corresponding control mode is stored in the register 107
in a step F2200, and the corresponding control timing is
10 stored in the register 108. The steps F2100, F2200 and
F2300 are repeated until the result of decision in the
step F2100 becomes "YES", and the program F2000 comes to
its end.

In Fig. 12, a loop flow is shown for
15 illustrating the outline of the program F2000. Actually,
however, the program F2000 includes series flows as shown
in Fig. 13. Therefore, the program F2000 for setting and
executing a control mode will be described in further
detail with reference to Fig. 13.

20 The flow chart of Fig. 13 corresponds to the
control mode M1 shown in Fig. 5 in which the value of the
composite phase θ_T is included within the range of 0° to
 60° . As described already, the control mode M1 shown in
Fig. 5 includes the control step 1 ranging from time $t =$
25 t_0 to time $t = \Delta t_1 + t_0$, and the control step 2 ranging
from time $t = \Delta t_1 + t_0$ to time $t = 2 \cdot \Delta t_1 + t_0$.

First, decision is made in a step F2001 shown in
Fig. 13 as to whether the present processing is to be

1 directed to the control step 1 or step 2. According to
the result of decision in the step F2001 and instructions
given in later steps F2006 and F2011, the control step 1
and control step 2 are basically alternately repeated.

5 Suppose now, for example, that the result of decision in
the step F2001 is "YES". In this case, a step F2002 is
executed. This step F2002 is scheduled to provide the
pulse pattern for immediately turning on the transistors
54, 55, 56 and immediately turning off the transistors 51,
10 52, 53. Then, a step F2003 is executed which is scheduled
to turn on the transistor 53 and turn off the transistor
56 after the period of time t_3 . Then, a step 2004 is
executed which is scheduled to turn on the transistor 51
and turn off the transistor 54 after the period of time
15 t_1 . Then, a step F2005 is executed which is scheduled
to turn on the transistor 52 and turn off the transistor
55 after the period of time t_2 . Then, in a step F2006,
an instruction instructing execution of schedules of the
control step 2 in the next processing which starts at time
20 $t = \Delta t_1 + t_0$.

On the other hand, the step F2001 is "NO", a
step F2007 is executed which is scheduled to immediately
turn on the transistors 51, 52, 53 and immediately turn
off the transistors 54, 55, 56. Then, a step F2008 is
25 executed which is scheduled to turn on the transistor 55
and turn off the transistor 52 after the period of time
 t_5 . Then, a step F2009 is executed which is scheduled
to turn on the transistor 54 and turn off the transistor

1 51 after the period of time t_4 . Then, a step F2010 is
executed which is scheduled to turn on the transistor 56
and turn off the transistor 53 after the period of time
 t_6 . Finally, in a step F2011, an instruction instruct-
5 ing execution of the schedules of the control step 1 in
the next processing is given, and the program F2000 comes
to its end.

The operation in the case of the control mode M1
has been described with reference to Fig. 13, by way of
10 example. It is apparent that, in the other control modes,
the corresponding transistors turned on and off in the
steps F2002 to F2005 and F2007 to F2010 change as shown in
the table of Fig. 14. Therefore, six kinds of processing
programs similar to that described with reference to Fig.
15 13 are cyclically executed while changing over the
transistors in each control mode as seen in Fig. 14. The
table shown in Fig. 14 is stored in the ROM 103 of the
microcomputer 10.

Fig. 15 shows an example of the PWM control
20 pulse pattern obtained by the above manner of control
according to the present invention. It will be apparent
from Fig. 15 that the pulse pattern includes changing
pulse widths providing a waveform sufficiently close to a
sinusoidal waveform.

25 In the embodiment of the present invention
described above, the processing program comprises the
steps of computing the composite phase θ_T , determining
the transistors to be turned on/off on the basis of the

1 computed composite phase θ_T , determining the on/off
timing of the transistors on the basis of the phase θ_T
too, and finally scheduling the combination of the
transistors to be turned on/off and the timing of
5 controlling those transistors. The processing program
described above is sequentially repeated at the time
interval of the predetermined constant period of time
 Δt_1 . Therefore such a manner of sequential processing
is advantageous over the prior art method of comparing
10 modulation wave with carrier wave in that not only the
microprocessor is freed from being always restrained for
the signal comparison purpose, but also the inverter can
generate an output waveform close to a sinusoidal waveform
because of the effect of the pulse pattern control.

15 In the aforementioned embodiment of the present
invention, the frequency command ω_1^* and the phase
command θ^* are used to compute the composite phase θ_T
taking into consideration the vector control of the
induction motor. However, in the case where application
20 of the inverter frequency command ω_1^* only is required,
and the phase command θ^* need not be applied, the
composite phase θ_T can be computed according to the
equation

$$\theta_T = \Sigma \omega_1^* \Delta t$$

without impairing the essence of the present invention.

25 Further, the programmable I/O function in the

1 one-chip microcomputer 10 shown in Fig. 1 is utilized for
the execution of scheduled processing in the control mode
setting and execution program F2000 shown in Fig. 13.
However, when the capacity of the input and output ports
5 101 and 106 is insufficient or when the programmable I/O
function in the one-chip microcomputer 10 cannot be used
due to the necessity of, for example, checking the port
output signals, an external peripheral I/O equipment
having an equivalent function may be used to exhibit the
10 effect similar to that described above.

The foregoing description has not referred in
detail to a change in the timer interrupt time interval
 Δt_1 . However, in the case of an application where the
switching frequency must be changed due to an external
15 factor such as a temperature rise of the switching
elements, any change in the time interval Δt_1 can be
dealt with by merely adding a routine in which the pulse
width is changed in proportion to such changes in the
external factors.

20 In the aforementioned embodiment of the present
invention, the a.c. output of the inverter is supposed to
have a sinusoidal waveform, and, on the basis of the above
supposition, the modulation wave signal having a purely
sinusoidal waveform is used. However, when the main
25 switching elements (the transistors in the case of the
illustrated embodiment) used in the inverter require a
relatively long dead time for preventing an undesirable
short-circuit trouble, use of the modulation wave signal

- 1 having the purely sinusoidal waveform would not always
bring the best result.

In such a case, a modified sine wave signal
modified by adding, for example, a positive bias and a
5 negative bias to the sine wave signal to an interval of an
electrical angle of 180° , or a modified sine wave signal
obtained by adding and subtracting bias components to and
from the sine wave signal after retrieval of the sine wave
signal may be used as the modulation wave signal, so that
10 the resultant a.c. output of the inverter has a sinusoidal
waveform.

It will be understood from the foregoing
detailed description of the present invention that a PWM-
controlled voltage source inverter can be controlled
15 according to a software program in a manner entirely
different from the prior art method of comparing modula-
tion wave with carrier wave. Therefore, the control
circuit can be made smaller in scale, while, at the same
time, the high reliability and accuracy of the operation
20 of the control circuit can be further improved.



CLAIMS:

1. A control apparatus generating a control signal for controlling the conduction state of a plurality of switching elements in a PWM-controlled voltage source inverter converting a d.c. power input into a polyphase a.c. power output, comprising:
 - a) means responsive to a given desired value of the a.c. output of said inverter for determining an inverter output phase command value corresponding to said desired value;
 - b) control mode selecting means responsive to said phase command value for selecting a control mode specifying the order of controlling said plural switching elements from among a plurality of control modes;
 - c) means for determining control timing for said switching elements to be controlled in the order specified by said control mode selected in response to said phase command value, said control timing determining means including means for generating a modulation wave signal corresponding to each phase of said polyphase a.c. power, means for setting a first reference value having a level high by a predetermined value than the level of the positive peak value of said modulation wave signal of each phase and a second reference value having a level lower than the level of the negative peak value of said modulation wave signal of each phase, means for setting the difference between said first reference value and the instantaneous value of said modulation wave signal of each



phase at said phase command value as first control timing for said switching elements, and means for setting the difference between said second reference value and the instantaneous value of said modulation wave signal of each phase at a value, which is the sum of said phase command value and a predetermined phase value, as second control timing succeeding said first control timing; and

d) means for generating a control signal to control said switching elements on the basis of said selected control mode and said first and second control timing settings, said control signal generating means further including timer means generating an output representing the real time, comparing means generating a coincidence signal when coincidence is detected between the real time output of said timer means and said first or second control timing setting, and output means responsive to said coincidence signal for applying said control signal at said control timings to said switching elements to be controlled in the order specified by said selected control mode.

2. A method for generating a control signal for controlling the conduction state of a plurality of switching elements in a PWM-controlled voltage source inverter converting a d.c. power input into a polyphase a.c. power output, comprising the steps of:

a) determining an inverter output phase command value corresponding to a given desired value of the a.c. output of said inverter;



b) selecting, in response to said phase command value, a control mode specifying the order of controlling said plural switching elements from among a plurality of control modes;

c) determining control timing for said switching elements to be controlled in the order specified by said control mode selected in response to said phase command value, said control timing determining step including generating a modulation wave signal corresponding to each phase of said polyphase a.c. power, setting a first reference value having a level higher by a predetermined value than the level of the positive peak value of said modulation wave signal of each phase and a second reference value having a level lower by a predetermined value than the level of the negative peak value of said modulation wave signal of each phase, setting the difference between said first reference value and the instantaneous value of said modulation signal of each phase at said phase command value as first control timing for said switching elements, and setting the difference between said second reference value and the instantaneous value of said modulation wave signal at a value, which is the sum of said phase command value and a predetermined phase value, as second control timing succeeding said first timing; and

d) generating a control signal to control said switching elements on the basis of said selected control mode and said first and second control timing settings,



said control signal generating step further including generating a coincidence signal when coincidence is detected between the real time and said first or second control timing, and, in response to said coincidence signal, applying said control signal at said control timings to said switching elements to be controlled in the order specified by said selected control mode.

3. A method according to Claim 2, wherein said first control timing and said second control timing are alternately set.

4. A method according to Claim 2, wherein said predetermined phase value is determined by the following equation:

$$\int \omega^*_{l(n+1)} dt + \theta^*_{(n+1)} - \theta^*_{(n)}$$

where $\omega^*_{l(n+1)}$ represents a frequency command signal, $\theta^*_{(n+1)}$ represents a present phase command signal and $\theta^*_{(n)}$ represents a former phase command signal.

5. A method according to Claim 4, wherein said predetermined phase value used for setting said second control timing is selected to be zero.

6. A method according to Claim 5, wherein said phase command value is given by the sum of a value obtained by integrating a desired frequency command value of the inverter output at a time interval of a unit time and said desired phase command value of the inverter output.



7. A method according to Claim 4, wherein the absolute value of said first reference value and that of said second reference value are selected to be equal to each other.
8. A method according to Claim 7, wherein the absolute values of said first and second reference values are selected to be equal to a half period of time corresponding to said predetermined phase value.
9. A method according to Claim 4, wherein said step of selecting said control mode includes the step of making reference to a previously prepared table showing a correspondence between said switching elements to be turned on/off at said first and second control timings and said plural control modes specifying the order of controlling said switching elements.
10. A method according to Claim 4, wherein, in said step of selecting said control mode, a different one of said plural control modes is selected whenever said phase command value is changed by an electrical angle of 60° .
11. A method according to Claim 5, wherein said second control timing setting is obtained by subtracting said first control timing setting from a predetermined period of time.
12. A method according to Claim 11, wherein said phase command value is determined at a time interval of a period of time which is twice as long as said predetermined period of time.
13. A method according to Claim 12, wherein said



phase command value is given by integrating said desired frequency value of the inverter output at a time interval of said predetermined period of time.

14. A method according to Claim 13, wherein said predetermined period of time is variable.

15. A method according to Claim 4, wherein the absolute values of said first and second reference values are selected to be different from each other.
