WHAT IS CLAIMED IS:

1. An apparatus comprising:

a circuit configured to:

receive a first phase control value of a phase control value signal;

generate a first phase interpolator control signal value of a phase interpolator control signal;

generate a first digital interpolator control signal value of a digital interpolator control signal;

phase interpolate a clock signal based on the first phase interpolator control signal value to produce a phase shifted clock signal; and

digitally interpolate a digital sample based on the first digital interpolator control signal value to produce a phase shifted digital sample having an effective phase based on the first phase control value, the digital sample generated using the phase shifted clock signal as a sample clock.

2. The apparatus of claim 1, further comprising the circuit further including an analog-to-digital converter (ADC) and the ADC being configured to sample an input signal based on the phase shifted clock signal to produce digital samples including the digital sample.

3. The apparatus of claim 2, further comprising the circuit further configured to perform the generation of the phase interpolator control signal by stepping the phase interpolator control signal on a per period basis toward the current value of the phase control value signal for a current sample period.

4. The apparatus of claim 3, further comprising the circuit further configured to perform the stepping of the phase interpolator control signal toward the current phase control value by:

determining a difference between a current value of the phase interpolator control signal and the current phase control value;

performing error unwrapping on the difference to produce an unwrapped difference; and

performing error saturation on the unwrapped difference based on a phase step size to produce an unwrapped saturated difference; and

updating the current value of the phase interpolator control signal based on the unwrapped saturated difference and the current value of the phase interpolator control signal.

5. The apparatus of claim 3, wherein :

the first phase interpolator control signal value is generated based on a second phase control value received in a first sample period a delay period before a second sample period in which the first phase control value was received.

6. The apparatus of claim 3 further comprising:

a buffer that buffers phase interpolator control signal values for at least a delay period; and

the circuit is configured to perform the digital interpolation of digital samples generated by the ADC based on the digital interpolator control signal to produce phase shifted digital samples, the digital interpolator control signal being generated based on a difference of a current phase control value and a phase interpolator control signal value generated in a sample period a delay period before a first current sample period.

7. The apparatus of claim 6, further comprising a digital receiver that processes the phase shifted digital samples, a logic of the digital receiver being clocked based on the phase shifted clock signal.

8. The apparatus of claim 7, further comprising the digital receiver being one of a decoder, a filter or a detector.

9. The apparatus of claim 7, further comprising the digital receiver further configured to generate the phase control signal.

10. A system comprising:

a timing control circuit configured to:

receive a first phase control value of a phase control signal;

generate a phase interpolator control signal based on the phase control signal;

generate a first digital interpolator control signal value of a digital interpolator control signal based on the phase control signal;

a phase interpolator that phase interpolates a clock signal based on the phase interpolator control signal to produce a phase shifted clock signal; and

a digital interpolator that digitally interpolates digital samples based on the digital interpolator control signal to produce phase shifted digital samples; a first digital sample of the digital samples being interpolated based on a first digital interpolator control value of the digital interpolator control signal to produce a first phase shifted digital sample having an effective phase based on the first phase control value, the digital samples being generated using the phase shifted clock signal as a sample clock.

11. The system of claim 10 further comprising:

an analog-to-digital converter (ADC) configured to sample an input signal based on the phase shifted clock signal to produce the digital samples.

12. The system of claim 11 further comprising the timing control circuit further configured to:

perform the generation of the phase interpolator control signal by stepping the phase interpolator control signal on a per period basis toward the current value of the phase control signal for a current sample period.

13. The system of claim 12 further comprising the timing control circuit further configured to perform the stepping of the phase interpolator control signal toward the current phase control value by:

determining a difference between a current value of the phase interpolator control signal and the current phase control value;

performing error unwrapping on the difference to produce an unwrapped difference;

performing error saturation on the unwrapped difference based on a phase step size to produce an unwrapped saturated difference; and

updating the current value of the phase interpolator control signal based on the unwrapped saturated difference and the current value of the phase interpolator control signal.

14. The system of claim 12 wherein: the timing control circuit is further configured for generating a first phase interpolator control value based on a second phase control value received in a first sample period a delay period before a second sample period in which the first phase control value was received; and

the first digital sample is generated using the phase shifted clock signal as phase interpolated using the first phase interpolator control value as a sample clock.

15. The system of claim 12 further comprising:

a buffer that buffers values of the phase interpolator control signal for at least a delay period; and

the digital interpolator control signal being generated based on a difference of a current phase control value and a phase interpolator control signal value generated the delay period before a current sample period.

16. The system of claim 10 further comprising a digital receiver that processes the phase shifted digital samples, a logic of the digital receiver being clocked based on the

phase shifted clock signal and the digital receiver being configured to generate the phase control signal.

17. A method comprising:

receiving, by a timing control circuit, a first phase control value of a phase control value signal;

generating, by the timing control circuit, a first phase interpolator control signal value of a phase interpolator control signal;

generating, by the timing control circuit, a first digital interpolator control signal value of a digital interpolator control signal;

phase interpolating a clock signal based on the first phase interpolator control signal value to produce a phase shifted clock signal; and

digitally interpolating a digital sample based on the first digital interpolator control signal value to produce a phase shifted digital sample having an effective phase based on the first phase control value, the digital sample generated using the phase shifted clock signal as a sample clock.

18. The method of claim 17 further comprising

performing the generation of the phase interpolator control signal by stepping the phase interpolator control signal on a per period basis toward the current value of the phase control value signal for a current sample period by:

determining a difference between a current value of the phase interpolator control signal and the current phase control value;

performing error unwrapping on the difference to produce an unwrapped difference;

performing error saturation on the unwrapped difference to produce a unwrapped saturated difference; and

updating the current value of the phase interpolator control signal based on the unwrapped saturated difference and the current value of the phase interpolator control signal.

19. The method of claim 18 further comprising generating the first phase interpolator control value based on a second phase control value received in a sample period a delay period before a second sample period in which the first phase control value was received.

20. The method of claim 19 further comprising generating the digital interpolator control signal based on a difference of the first phase control value and the first phase interpolator control signal value.