



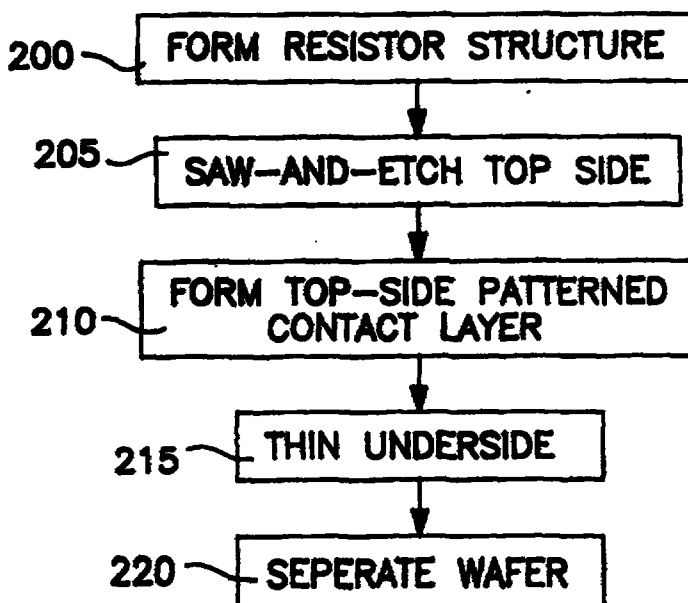
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(21) International Application Number: PCT/US95/06929 (22) International Filing Date: 1 June 1995 (01.06.95) (30) Priority Data: 08/257,726 9 June 1994 (09.06.94) US (71) Applicant: MICRO TECHNOLOGY PARTNERS [US/US]; 576 Charcot Avenue, San Jose, CA 95131 (US). (72) Inventors: RICHARDS, John, G.; 4847 Tonino Drive, San Jose, CA 95136 (US). FLORES, Hector; 1911 Lanai Avenue, San Jose, CA 95122 (US). (74) Agents: VINCENT, Lester, J. et al.; Blakely, Sokoloff, Taylor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025-1026 (US).	(81) Designated States: AM, AT, AT (Utility model), AU, BB, BG, BR, BY, CA, CH, CN, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, ES, FI, FI (Utility model), GB, GE, HU, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LT, EU, LV, MD, MG, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), TJ, TM, TT, UA, UG, UZ, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG), ARIPO patent (KE, MW, SD, SZ, UG). Published <i>With international search report.</i> 9611871-6 ✓ RTMP copy	

(54) Title: RESISTOR FABRICATION

(57) Abstract

The fabrication of a resistor structure is described. A resistive region (103) is formed over the top of a substrate (106). Trenches are formed from the top side of the substrate in scribe line regions where the wafer is to be separated to form resistor modules. Contact layers (141, 142) are formed over the top side of the substrate (106) and are electrically coupled to each end of the resistive region (103), respectively. The contact layers (141, 142) are also formed over the sidewalls of the trenches. The wafer is separated through the trenches, creating resistor modules having sidewall contact regions.



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