

DOUBLE-SIDED POLISHING METHOD FOR LARGE-SIZE ULTRATHIN LITHIUM NIOBATE SUBSTRATE

Description

Double-sided polishing method for a large-size ultra-thin lithium niobate substrate

Technology background

This invention involves semiconductor material field, in particular to the double-sided polishing method for lithium niobate substrate used as semiconductor substrate.

Background technology

Lithium niobate (LiNbO_3 , hereinafter referred to as LN) is a kind of multifunctional material with piezoelectric, ferroelectric, pyroelectric, nonlinear, photoelectric, photo elastic, photorefractive functions. With its excellent physical properties, LN is getting more and more attention and is widely applied in the fields of aviation, space, civil photoelectric products. Double-sided polished LN substrate is widely applied in sensors, acousto-optic devices, optical gyroscopes, etc. Different from silicon crystal and sapphire crystal, LN is characterized by extreme low fracture toughness and hardness. For example, its fracture toughness is about one-third of silicon's and one-tenth of sapphire's. Large-size Ultra-thin LN substrate could be easily broken during processing, which makes high rejection rate, low processing efficiency and high cost.

With the development and progress of IC design and manufacturing technology, the integration of IC continuously improves with the trend of exponentially growing chip density, shrinking line width, increasing line density, flattening focus depth. Device goes into the direction of miniaturization and chip, which requires the substrate material to be large-size and ultra-thin, meanwhile the requirements for the roughness and flatness of the substrate material get higher. Polishing technology is always an important method of ultra-precision machining to lower surface roughness, remove the damage layer and achieve smooth surface without damage. Ultra-precision CMP has already been recognized by the industry as the most efficient technology for global planarization of the wafer in semiconductor manufacturing.

Under normal polishing condition, material removal rate is proportional to polishing speed, polishing pressure and polishing temperature. The higher polishing speed, pressure and temperature, the higher material removal rate, which would result in higher surface roughness. Meanwhile, Non-uniformity of polishing positive pressure would result in uneven wear in polishing, which would deteriorate polishing quality, making roughness and flatness worse.

Invention content

The technical problem which needs to be solved by this invention is to provide a double-side polishing method for large-size ultra-thin lithium niobate substrate which makes one-time polishing in bulk production, making high polishing efficiency, high surface flatness of LN substrate. The feature of the polishing method makes LN substrate unbreakable during device application with high material utility and high rate of processed products.

The technical scheme to solve the technical problem adopted by this invention is: a double-sided polishing method for a large-size ultra-thin lithium niobate substrate which includes the steps as follows:

Lap the large-size ultra-thin LN wafer after slicing with the abrasive of particle size $1\mu\text{m}\sim 16\mu\text{m}$, making large-size ultra-thin LN wafer's roughness $<200\text{nm}$, flatness $<10\mu\text{m}$. And then make ultrasonic cleaning, obtaining large-size ultra-thin double-side lapped LN wafer with surface coarse structure;

b) Double-side thin large-size ultra-thin LN wafer after lapping with the abrasive of particle size 2000# $\sim$ 10000# by special thin grinding wheel, making large-size ultra-thin LN wafer's roughness $<100\text{nm}$, flatness $<2\mu\text{m}$. And then make ultrasonic cleaning, obtaining large-size ultra-thin double-side thinned LN wafer with surface coarse structure;

c) Corrode large-size ultra-thin double-side thinned LN wafer in closed container which containing uniform mixing nitric acid, hydrofluoric acid and relievers under the conditions of corrosion temperature $20^{\circ}\text{C}\sim 25^{\circ}\text{C}$, corrosion time 12 $\sim$ 48 hours, making large-size ultra-thin LN wafer's roughness $<50\text{nm}$, flatness $<2\mu\text{m}$. And then make ultrasonic cleaning, obtaining large-size ultra-thin LN corroded wafer with random and disordered pit structure on the surface;

d) Double-side polish the large-size ultra-thin LN corroded wafer with double-side polisher and polishing liquid under the conditions of polishing unit pressure $200\text{g}/\text{cm}^2 \sim 1400\text{g}/\text{cm}^2$, polishing temperature $20^{\circ}\text{C} \sim 25^{\circ}\text{C}$, making large-size ultra-thin LN wafer's roughness $<0.50\text{nm}$, flatness $<1\mu\text{m}$, the lateral dimension of the indentation $0.10\mu\text{m}\sim 0.30\mu\text{m}$, vertical depth $0.10\text{nm}\sim 0.50\text{nm}$, 20% $\sim$ 80% of the surface area of large-size ultra-thin LN substrate occupied by the depression. And then make ultrasonic cleaning, obtaining final large-size ultra-thin double-side polished LN wafer.

As an option, in the mentioned Step a, the thickness of LN AS wafer is $200\mu\text{m}\sim 250\mu\text{m}$, the thickness of double-side lapped LN wafer is $170\mu\text{m}\sim 220\mu\text{m}$, the thickness of double-side thinned LN wafer is $160\mu\text{m}\sim 210\mu\text{m}$.

As an option, the mentioned abrasive is a mixture of one or more materials which includes boron carbide, diamond, alumina or silicon carbide. The roughness of lapped LN wafer is

depended by the particle size of the silicon carbide abrasive. Normally, bigger particle size makes bigger roughness.

Double-side thinning mentioned in the above step b) means, apply double-side small grain grinding wheel to thin large-size ultra-thin double-side lapped LN wafer to control flatness and warpage, reduce the damage layer of double-side lapped LN wafer and polishing time.

Chemical corrosion mentioned in the above step c) means, etch leveling lapped LN substrate in mixed acid, removal of surface impurities, surface damage repair and warpage control.

Corrosive liquid mentioned in the above step c) is a mixture of one or more of HNO_3 , HF and relievers.

As mentioned in the above step c), corrosion time is determined by the flatness and warpage of LN wafer after polishing, which may range from few minutes to dozens of hours. 12~48 hours is recommended. Chemical corrosion could be finished when warpage $< 25\mu\text{m}$, roughness $< 50\text{nm}$, flatness $< 2\mu\text{m}$. After chemical corrosion, the substrate would achieve local flattening with random and disordered pit structure on the surface.

As mentioned in the above step d), the formation process of polished surface is complex. The processing in the initial phase is to remove tiny bulges left from the former process. The real polishing area in this phase is tiny, and polishing pressure per unit area is huge, so the rate of formation of polished surface is high. As the polishing process goes on, polished surface area of the wafer increases, and polishing pressure per unit area and the rate of formation of polished surface decline. The processing in this phase is to polish the whole surface. The third phase takes the longest time in the whole polishing process. Most of the polished surface has been formed in the second phase, so the main task in this phase is to remove some large defects on the surface of the wafer, which would take at least double time to achieve this target.

Double-sided polishing method for a large-size ultra-thin LN substrate mentioned in this invention owns roughness of the polished surface $< 0.50\text{nm}$, flatness $< 1\mu\text{m}$, and a random and disordered pit structure on the surface. LN substrate with random and disordered pit structure on the surface mentioned in this invention owns $0.10\mu\text{m} \sim 0.30\mu\text{m}$ lateral dimension of the indentation, $0.10\text{nm} \sim 0.50\text{nm}$ vertical depth and 20%~80% of the surface area of large-size ultra-thin LN substrate occupied by the depression.

Polishing pressure mentioned in this invention has a great impact on polishing rate and the quality of the polished surface. Usually the polishing pressure increases, the mechanical action increases, and the polishing rate also increases. However, exorbitant polishing pressure would result in uneven polishing rate, the abrasion of the polishing pad and the area temperature increase, which is hard to control. That would make increased probability of scratches, fragmentation and edge clips etc. on large-size ultra-thin wafer, which reduce polishing quality and raise the cost.

Comparison with the traditional global planarization LN substrate.

First, compared with traditional two-sided rough and fine polishing technology, one-time polishing of large-size ultra-thin LN substrate mentioned in this invention greatly reduces the rate of defective products and processing costs. Meanwhile, double-sided polishing method for a large-size ultra-thin LN substrate mentioned in this invention adopts CMP technology, which makes it possible to apply one-time polishing on a mass of double-side thinned LN wafers, greatly raising polishing efficiency.

Second, the surface roughness of LN substrate mentioned in this invention is small, which allows the direct application of such LN substrate in optical device; on the other hand, it could reduce internal stress caused by lattice mismatch in the back-end process, ease stress concentration, reduce dislocation density and raise the quality of back-end process LN substrate with random and disordered pit structure on the surface mentioned in this invention could enhance adhesion in the process of coating and coating, preventing from coating cracking; on the other hand, it could reduce internal stress caused by lattice mismatch in the back-end process, ease stress concentration, reduce dislocation density and raise the quality of optical device.

Third, the surface flatness of LN substrate mentioned in this invention is high, which determines the non-breakability, high material utility and high rate of processed products in device application.

Fourth, LN substrate mentioned in this invention is large-size and ultra-thin, which determines higher single input utilization rate in device application, meeting the demand for miniaturization and chip.

Instruction with pictures

Picture 1 is the sketch map which shows changes of the lateral dimension and vertical depth under different processing stress applied by this invention.

Picture 2 is the sketch map which shows changes of the roughness under different processing stress applied by this invention.

Picture 3 is the sketch map which shows changes of the flatness under different processing stress applied by this invention.

Hereinafter this invention is explained in further details with the sketch map.

Specific implementation mode

Hereinafter give specific examples to further elaborate this invention, please be kindly understand that these examples are not applied to restrain the scope of protection for this invention.

Implementation 1:

- a) Lap the large-size ultra-thin LN wafer after slicing with the abrasive of particle size $5\mu\text{m}$, making large-size ultra-thin LN wafer's roughness $<200\text{nm}$, flatness $<10\mu\text{m}$. And then make ultrasonic cleaning, obtaining large-size ultra-thin double-side lapped LN wafer with surface coarse structure;
- b) Double-side thin large-size ultra-thin LN wafer after lapping with the abrasive of particle size 6000# by special thin grinding wheel, making large-size ultra-thin LN wafer's roughness $<100\text{nm}$, flatness $<2\mu\text{m}$. And then make ultrasonic cleaning, obtaining large-size ultra-thin double-side thinned LN wafer with surface coarse structure;
- c) Corrode large-size ultra-thin double-side thinned LN wafer in closed container which containing uniform mixing nitric acid, hydrofluoric acid and relievers under the conditions of corrosion temperature $20^{\circ}\text{C}\sim 25^{\circ}\text{C}$, corrosion time $12\sim 48$ hours, making large-size ultra-thin LN wafers roughness $<50\text{nm}$, flatness $<2\mu\text{m}$. And then make ultrasonic cleaning, obtaining large-size ultra-thin LN corroded wafer with random and disordered pit structure on the surface;
- d) Double-side polish the large-size ultra-thin corroded LN wafer with double-side polisher and polishing liquid under the conditions of polishing unit pressure $300\text{g}/\text{cm}^2$, polishing temperature $20^{\circ}\text{C}\sim 25^{\circ}\text{C}$, making large-size ultra-thin LN wafer's roughness $<0.5\text{nm}$, flatness $<1\mu\text{m}$, the lateral dimension of the indentation $0.18\mu\text{m}$, vertical depth 0.39nm , $20\%\sim 80\%$ of the surface area of large-size ultra-thin LN substrate occupied by the depression. And then make ultrasonic cleaning, obtaining final large-size ultra-thin double-side polished LN wafer.

Implementation 2:

- a) Lap the large-size ultra-thin LN wafer after slicing with the abrasive of particle size $5\mu\text{m}$, making large-size ultra-thin LN wafer's roughness $<200\text{nm}$, flatness $<10\mu\text{m}$. And then make ultrasonic cleaning, obtaining large-size ultra-thin double-side lapped LN wafer with surface coarse structure;
- b) Double-side thin large-size ultra-thin LN wafer after lapping with the abrasive of particle size 6000# by special thin grinding wheel, making large-size ultra-thin LN wafer's roughness $<100\text{nm}$, flatness $<2\mu\text{m}$. And then make ultrasonic cleaning, obtaining large-size ultra-thin double-side thinned LN wafer with surface coarse structure;
- c) Corrode large-size ultra-thin double-side thinned LN wafer in closed container which containing uniform mixing nitric acid, hydrofluoric acid and relievers under the conditions of corrosion temperature $20^{\circ}\text{C}\sim 25^{\circ}\text{C}$, corrosion time $12\sim 48$ hours, making large-size ultra-thin LN wafer's roughness $<50\text{nm}$, flatness $<2\mu\text{m}$. And then make ultrasonic cleaning, obtaining large-size ultra-thin LN corroded wafer with random and disordered pit structure on the surface;

d) Double-side polish the large-size ultra-thin corroded LN wafer with double-side polisher and polishing liquid under the conditions of polishing unit pressure 400g/cm^2 , polishing temperature $20\sim 25^\circ\text{C}$, making large-size ultra-thin LN wafer's roughness $<0.5\text{nm}$, flatness $<1\mu\text{m}$, the lateral dimension of the indentation $0.15\mu\text{m}$, vertical depth 0.21nm , $20\%\sim 80\%$ of the surface area of large-size ultra-thin LN substrate occupied by the depression. And then make ultrasonic cleaning, obtaining final large-size ultra-thin double-side polished LN wafer.

Implementation 3:

a) Lap the large-size ultra-thin LN wafer after slicing with the abrasive of particle size $5\mu\text{m}$, making large-size ultra-thin LN wafer's roughness $<200\text{nm}$, flatness $<10\mu\text{m}$. And then make ultrasonic cleaning, obtaining large-size ultra-thin double-side lapped LN wafer with surface coarse structure;

b) Double-side thin large-size ultra-thin LN wafer after lapping with the abrasive of particle size 6000# by special thin grinding wheel, making large-size ultra-thin LN wafer's roughness $<100\text{nm}$, flatness $<2\mu\text{m}$. And then make ultrasonic cleaning, obtaining large-size ultra-thin double-side thinned LN wafer with surface coarse structure;

c) Corrode large-size ultra-thin double-side thinned LN wafer in closed container which containing uniform mixing nitric acid, hydrofluoric acid and relievers under the conditions of corrosion temperature $20^\circ\text{C}\sim 25^\circ\text{C}$, corrosion time $12\sim 48$ hours, making large-size ultra-thin LN wafer's roughness $<50\text{nm}$, flatness $<2\mu\text{m}$. And then make ultrasonic cleaning, obtaining large-size ultra-thin LN corroded wafer with random and disordered pit structure on the surface;

d) Double-side polish the large-size ultra-thin corroded LN wafer with double-side polisher and polishing liquid under the conditions of polishing unit pressure 500g/cm^2 , polishing temperature $20^\circ\text{C}\sim 25^\circ\text{C}$, making large-size ultra-thin LN wafer's roughness $<0.5\text{nm}$, flatness $<1\mu\text{m}$, the lateral dimension of the indentation $0.11\mu\text{m}$, vertical depth 0.13nm , $20\%\sim 80\%$ of the surface area of large-size ultra-thin LN substrate occupied by the depression. And then make ultrasonic cleaning, obtaining final large-size ultra-thin double-side polished LN wafer.

Implementation 4:

a) Lap the large-size ultra-thin LN wafer after slicing with the abrasive of particle size $5\mu\text{m}$, making large-size ultra-thin LN wafer's roughness $<200\text{nm}$, flatness $<10\mu\text{m}$. And then make ultrasonic cleaning, obtaining large-size ultra-thin double-side lapped LN wafer with surface coarse structure;

b) Double-side thin large-size ultra-thin LN wafer after lapping with the abrasive of particle size 6000# by special thin grinding wheel, making large-size ultra-thin LN wafer's roughness $<100\text{nm}$, flatness $<2\mu\text{m}$. And then make ultrasonic cleaning, obtaining large-size ultra-thin double-side thinned LN wafer with surface coarse structure;

c) Corrode large-size ultra-thin double-side thinned LN wafer in closed container which containing uniform mixing nitric acid, hydrofluoric acid and relievers under the conditions of corrosion temperature $20^{\circ}\text{C}\sim 25^{\circ}\text{C}$, corrosion time $12\sim 48$ hours, making large-size ultra-thin LN wafer's roughness $< 50\text{nm}$, flatness $< 2\mu\text{m}$. And then make ultrasonic cleaning, obtaining large-size ultra-thin LN corroded wafer with random and disordered pit structure on the surface;

d) Double-side polish the large-size ultra-thin corroded LN wafer with double-side polisher and polishing liquid under the conditions of polishing unit pressure $600\text{g}/\text{cm}^2$, polishing temperature $20\sim 25^{\circ}\text{C}$, making large-size ultra-thin LN wafer's roughness $< 0.5\text{nm}$, flatness $< 1\mu\text{m}$, the lateral dimension of the indentation $0.20\mu\text{m}$, vertical depth 0.32nm , $20\%\sim 80\%$ of the surface area of large-size ultra-thin LN substrate occupied by the depression. And then make ultrasonic cleaning, obtaining final large-size ultra-thin double-side polished LN wafer.

Claims

1. A double-sided polishing method for a large-size ultra-thin LN substrate includes the following steps:

a) lap the large-size ultra-thin LN wafer after slicing with a first abrasive of particle size $1 \sim 16 \mu\text{m}$, making large-size ultra-thin LN wafer's roughness $< 200 \text{nm}$, flatness $< 10 \mu\text{m}$, and then make ultrasonic cleaning, obtaining large-size ultra-thin double-side lapped LN wafer with surface coarse structure;

b) double-side thin large-size ultra-thin LN wafer after lapping with a second abrasive of particle size $2000\# \sim 10000\#$ by special thin grinding wheel, making large-size ultra-thin LN wafer's roughness $< 100 \text{nm}$, flatness $< 2 \mu\text{m}$ and then make ultrasonic cleaning, obtaining large-size ultra-thin double-side thinned LN wafer with surface coarse structure;

c) corrode large-size ultra-thin double-side thinned LN wafer in closed container which containing uniform mixing nitric acid, hydrofluoric acid and relievers under the conditions of corrosion temperature $20^\circ\text{C} \sim 25^\circ\text{C}$, corrosion time $12 \sim 48$ hours, making large-size ultra-thin LN wafer's warpage $< 25 \mu\text{m}$, roughness $< 50 \text{nm}$, flatness $< 2 \mu\text{m}$ and then make ultrasonic cleaning, obtaining large-size ultra-thin LN corroded wafer with random and disordered pit structure on the surface;

d) double-side polish the large-size ultra-thin LN corroded wafer with double-side polisher and polishing liquid under the conditions of polishing unit pressure $200 \text{g/cm}^2 \sim 1400 \text{g/cm}^2$, polishing temperature $20^\circ\text{C} \sim 25^\circ\text{C}$, making large-size ultra-thin LN wafer's roughness $< 0.50 \text{nm}$, flatness $< 1 \mu\text{m}$, the lateral dimension of the indentation $0.10 \mu\text{m} \sim 0.30 \mu\text{m}$, vertical depth $0.10 \text{nm} \sim 0.50 \text{nm}$, $20\% \sim 80\%$ of the surface area of large-size ultra-thin LN substrate occupied by the depression and then make ultrasonic cleaning, obtaining final large-size ultra-thin double-side polished LN wafer.

2. As mentioned in Claim 1, the features of the polishing method of large-size ultra-thin LN substrate are: the features of the polishing method of large-size ultra-thin LN substrate are: diameter $\geq 150 \text{mm}$, surface roughness $< 0.5 \text{nm}$, flatness $< 1 \mu\text{m}$, thickness is $150 \mu\text{m} \sim 200 \mu\text{m}$.

3. in the mentioned Step a, the thickness of large-size ultra-thin LN wafer after slicing is $200 \mu\text{m} \sim 250 \mu\text{m}$; the thickness of large-size ultra-thin double-side lapped LN wafer is $170 \mu\text{m} \sim 220 \mu\text{m}$.

4. As mentioned in Claim 1, the feature of the polishing method of large-size ultra-thin LN substrate is: in the mentioned Step a, the abrasive is a mixture of one or more materials which includes boron carbide, diamond, alumina or silicon carbide.

5. As mentioned in Claim 1, the feature of the polishing method of large-size ultra-thin LN substrate is: in the mentioned Step b, the thickness of large-size ultra-thin LN double-side thinned wafer is $160\mu\text{m}\sim 210\mu\text{m}$.

6. As mentioned in Claim 1, the feature of the polishing method of large-size ultra-thin LN substrate is: in the mentioned Step c, the warpage of large-size ultra-thin corroded LN wafer is $<25\mu\text{m}$.

7. As mentioned in Claim 1, the feature of the polishing method of large-size ultra-thin LN substrate is: in the mentioned Step d, the polishing liquid is alkaline silica or alumina.