Claims:

1. A method for producing a monolithic template comprising a Si wafer (having a diameter of up to 300 mm) with a layer of a III/V semiconductor epitaxially applied on a surface of the Si wafer, the III/V semiconductor having a lattice constant which differs by less than 10% from that of Si, comprising the following steps:

A) a layer of a III/V semiconductor is epitaxially applied on the surface of the Si wafer at a wafer temperature from 350 to 650 °C, a growth rate from 0.1 to 2 µm/h, and a layer thickness from 1 to 100 nm wherein the layer deposited in this step is deposited by Atomic Layer Deposition (ALD),

B) a layer of a III/V semiconductor, identically with or differently from the III/V semiconductor applied in step A), is epitaxially grown on the layer obtained in step A) at a wafer temperature from 500 to 800 °C, a growth rate from 0.1 to 10 µm/h, and a layer thickness from 10 to 150 nm.

2. The method according to claim 1, further including an etching step (before step A), wherein a Cl-containing gas is conducted over the surface at a wafer temperature from 600 to 1,200 °C for a time from 0 to 60 min at an etching rate from 0 to 5 µm/h.

3. The method according to claim 2, wherein prior to the etching step, the method further includes a deoxidizing step whereby the surface of the Si wafer is deoxidized, by baking out the wafer at a temperature from 800

to 1,200 °C for a time from 1 s to 30 min in an inert gas atmosphere.

4. The method according to claim 3, wherein prior to the etching step and after the deoxidizing step, the Si layer is epitaxially grown on the surface of the deoxidized Si wafer at a wafer temperature from 600 to 1,200 °C, at a growth rate from 0.01 to 20 µm/h, and wherein the layer thickness is from 0 to 5 µm.

5. The method according to any one of claims 1 to 4, wherein the surface of the Si wafer is a (001) Si surface with 0 to 6° misorientation in the direction <110>, wherein at a dislocation of ≤ 1° the direction of the dislocation can differ from <110>.

6. The method according to any one of claims 1 to 5, wherein in step A) a $Ga_xB_yAl_zP$ semiconductor is grown, wherein x = 0 - 1, y = 0 - 0.1 and z = 0 - 1, or w = 0 - 0.1 and v = 1 - w, wherein the sum of x, y and z is always 1.

7. The method according to any one of claims 1 to 5, wherein in step A) a GaN_wP_v semiconductor is grown, wherein x = 0 - 1, y = 0 - 0.1 and z = 0 - 1, or w = 0 - 0.1 and v = 1 - w.

8. The method according to any one of claims 1 to 6, wherein in step B) a $Ga_xB_yAl_zP$ semiconductor is grown, wherein x = 0 - 1, y = 0 - 0.1 and z = 0 - 1, or w = 0 - 0.1 and v = 1 - w, wherein the sum of x, y and z is always 1.

9. The method according to any one of claims 1 to 7, wherein in step B) a GaN_wP_v

semiconductor is grown, wherein x = 0 - 1, y = 0 - 0.1 and z = 0 - 1, or w = 0 - 0.1 and v = 1 - w.

10. The method according to any one of claims 1 to 9, wherein in step B) doping with Zn, Te, S, C, Mg and/or Si takes place in a p- or n-doping concentration of 10^{15} to 10^{21} cm^{-3}.

11. The method according to any one of claims 1 to 10, wherein in step B) doping with Zn, Te, S, C, Mg and/or Si takes place in a p- or n-doping concentration of 10^{15} to 10^{21} cm^{-3}.

12. The use of a template according to any one of claims 1-11, for the monolithic integration of III/V-based semiconductor components such as transistors, laser diodes, LEDs, detectors, and solar cells on a Si substrate, wherein the Si substrate, possesses a mask structure having a diameter of more than 6 cm.

13. The use of a template according to any one of claims 1-7, for the monolithic integration of III/V-based semiconductor components such as transistors, laser diodes, LEDs, detectors, and solar cells on a Si substrate, wherein the Si substrate, possesses a mask structure having a diameter of more than 10 cm.

14. The use of a template according to any one of claims 1-7, for the monolithic integration of III/V-based semiconductor components such as transistors, laser diodes, LEDs, detectors, and solar cells on a Si substrate, wherein the Si substrate, possesses

a mask structure having a diameter of more than 20 cm.

15. A monolithic template, obtainable by means of a method according to any one of claims 1 to 14.

16. The use of a template according to claim 15 in the manufacture of monolithic integration of III/V-based semiconductor components such as transistors, laser diodes, LEDs, detectors, and solar cells on a Si substrate, in particular on a Si substrate.

17. The use according to claim 16, wherein subsequently to step B), further III/V semiconductor layers are epitaxially grown, and electronic components comprising III/V semiconductor are formed.

Claims:

1. A method for producing a monolithic template comprising a Si wafer with a layer of a III/V semiconductor epitaxially applied on a surface of the Si wafer, the III/V semiconductor having a lattice constant, which differs by less than 10% from that of Si, comprising the following steps:

in a step B) performed before a step C) epitaxially growing a Si layer on the surface of the Si wafer at a wafer temperature from 600 to 1200 °C, growth rate 0.01-20 µm/h, and thickness of the Si layer up to 5 µm;

in the step C) performed before a step D) an active Cl-containing gas is conducted over a surface of the Si layer at a wafer temperature from 600 to 1,200 °C for a time up to 60 min for etching at an etching rate up to 5 µm/h;

in the step D) epitaxially growing a layer of the III/V semiconductor on the surface of the Si layer at a wafer temperature from 350 to 650°C, a growth rate from 0.1 to 2 µm/h, and a layer thickness from 1 to 100 nm;

in the step E) after the step D) epitaxially growing a layer of a III/V semi-conductor, identical to or different from the III/V semiconductor grown in the step D) at a wafer temperature from 500 to 800°C, a growth rate from 0.1 to 10 µm/h, and a layer thickness from 10 to 150 nm.

2. The method according to claim 1, wherein step A) is carried out before step B) by baking-out the surface of the Si wafer to a wafer temperature from 800 to 1,200 °C for a time from 1 s to 30 min in an inert gas atmosphere.

3. The method according to claim 1, wherein in the step D) the layer is epitaxially grown by atomic layer deposition (ALD).

4. The method according to claim 1, wherein the surface of the Si wafer is a (001) Si surface with 0 to 6° misorientation in the direction <110>.

5. The method according to claim 1, wherein the III/V semiconductor grown in the step D) semiconductor is a $Ga_xB_yAl_zP$, wherein x = 0 - 1, y = 0 - 0.1 and z = 0 - 1, wherein the sum of x, y and z for $Ga_xB_yAl_zP$ is always 1.

6. The method according to claim 1, wherein the III/V semiconductor grown in the step D) is a $GaN_w P_v$ semiconductor, wherein, w = 0 - 0.1 and v = 1 - w.

7. The method according to claim 1, wherein the III/V semiconductor grown in the step E) semiconductor is a $Ga_xB_yAl_zP$, wherein x = 0 - 1, y = 0 - 0.1 and z = 0 - 1, wherein the sum of x, y and z for $Ga_xB_yAl_zP$ is always 1.

8. The method according to claim 1, wherein the III/V semiconductor grown in the step E) is a $GaN_w P_v$ semiconductor, wherein, wherein w = 0 -0.1 and v = 1 - w.

9. The method according to claim 1, wherein the III/V semiconductor grown in the step D) is doped with Zn, Te, S, C, Mg and/or Si at a doping concentration of 10^{15}-10^{21} cm^3.

10. The method according to claim 1, wherein the III/V semiconductor grown in the step E) is doped with Zn, Te, S, C, Mg and/or Si at a doping concentration of 10^{15}-10^{21} cm^3.

11. The method of claim 1, wherein the substrate diameter is greater than 6 cm.

12. The method of claim 1, wherein the substrate diameter is greater than 10 cm.

13. The method of claim 1, wherein the substrate diameter is greater than 20 cm.