

Description

This invention relates to apparatus for and methods of protecting a system against corruption or loss of output signal due to a malfunction.

In diverse technical areas that rely on reliable communication of signals, such as telephony and data transmission and switching, data processing, and process control, it is common to duplicate—or even more extensively replicate—system components (e.g., control units, circuit packs) in order to achieve fault tolerance, and hence reliability.

The replicated components typically operate either in active mode (all components are simultaneously operating in the same state and using the same inputs), or in "hot" standby mode (all components are powered up, but are not necessarily in the same state nor using the same inputs), or in "cold" standby mode (the non-active components need not be powered up).

When using standby components, some form of testing of the active component, or error detection in the data stream(s) processed by the active component, is typically used to determine when a switch of system output (a "protection switch") should be made from the active component to a standby component. Irrespective of whether the standby component is hot or cold, however, the switching action conventionally results in a time period during which data is corrupted.

Alternatively, having the replicated components operate in synchronized active mode can prevent data corruption if three or more components are used (e.g., by "voting" to determine the system output). However, having such redundancy has other problems. These problems include the cost of the extra component(s), increased probability of internal failure (because there is more equipment to fail) and the associated increased maintenance cost, and the extra space and wiring required to accommodate the extra component(s). Therefore, it would be advantageous to have an arrangement which would use only two replicated active components, but which would retain the ability to prevent data corruption.

Additionally, arrangements such as voting, which operate on the possible output signals themselves in order to determine which one should become the system output, introduce the possibility that the arrangements themselves will corrupt the output data which they are intended to safeguard.

Digitized voice is relatively tolerant of data corruption. And, for low-speed data, if the time during which data is corrupted as a result of protection switching could be made less than a bit time, either error correction schemes or error detection combined with minimal retransmission could be used effectively to prevent corruption. However, for high-speed data, protection switching causes burst errors which make

correction schemes impractical and detection schemes less reliable. Further, these burst errors may last long enough to corrupt the data of more than one user. If a burst error is not detected, myriad problems arise. Even when a burst error is detected, retransmission is needed, and it typically must be invoked either manually or by higher layers of data protocol. Thus, with a grade of service that allows error bursts caused by protection switching, upgrading of the equipment to operate with the protocol options that automate retransmission would normally be required. This may be very costly for high-speed data systems. Also, retransmission following a protection switch may cause temporary overload conditions. For these reasons, the prevention of data corruption rather than the mere curing of corrupted data is more desirable for high-speed data switching communication services.

According to one aspect of this invention there is provided apparatus as claimed in claim 1.

According to another aspect of this invention there is provided a method as claimed in claim 17.

The invention is directed to solving the data corruption problem of the prior art while offering the option of having duplicated—as opposed to more extensively replicated—components.

Specifically an arrangement may be provided for use with replicated signal-handling components—be they transmission links, switching nodes, processors, or any other equipment—which eliminates the previously-described corruption of output. The arrangement uses either an error detection mechanism connected to the outputs of the signal-handling components to detect errors in the output of any of the components, or a fault detection mechanism connected to the components themselves to detect faulty operation of any of the components. The preferred implementation employs error detection on the outputs, as this will detect not only the effects of faults, but also other errors such as noise-induced transient errors, and because the time it takes to detect an error is typically small. For purposes of this application, both faults in components and errors in component outputs will be subsumed in the term "malfunction." The malfunction detection mechanism generates a malfunction signal to indicate detection of a malfunction at any of the signal-handling components.

A signal delay arrangement is connected to the outputs of the signal-handling components. The delay arrangement receives the output signals of the components and outputs them following a delay of time sufficient for the malfunction-detection mechanism to detect a malfunction and to generate the malfunction signal. A system output signal generating arrangement is connected to the delay arrangement to receive therefrom the delayed output signals. The generating arrangement outputs a system output signal which corresponds to at least one of the received

delayed signals. However, the generating arrangement responds to the malfunction signal to output a system output signal which corresponds only to received delayed signals which are not affected by the malfunction. That is, the malfunction signal serves to block a delayed output signal which is affected by the detected malfunction from being used in generating the system output signal, while the delay arrangement provides sufficient time for the malfunction to be detected and the requisite blocking to commence.

The above characterization makes clear that no output information is corrupted or lost as a result of the output of one or more of the replicated components becoming faulty and system output switching, as a consequence, to being based on non-faulty outputs. No loss or corruption results because the output signal delay introduced by the delay arrangement equals or exceeds the time needed to detect the error condition and to effect the blocking of the errored signal. Furthermore, the signals on which the system output will be based are not directly operated on by the malfunction-detection mechanism, but are propagating through the delay mechanism while malfunction detection occurs. Hence, the arrangement is not likely to itself be a corruptor of the system output.

To further limit the possibility that the arrangement itself would bring about failure of a system that uses it, it is desirable to make as many parts thereof as possible out of passive elements. The signal delay arrangement and the system output signal generating arrangement are particularly suited for implementation from passive parts, particularly from passive optical parts. For example, the delay arrangement may comprise lengths of optical fiber, and the generating arrangement may comprise optical AND gates (e.g., transphasors), for selectively passing-through or blocking component output signals. The outputs of the AND gates may further be combined into a single output by means of an optical OR gate (e.g., a coupler) or another optical AND gate.

These and other advantages of the present invention will become apparent from the following description of an illustrative embodiment of the invention considered together with the drawing.

Brief Description of the Drawing

FIG. 1 shows in block diagram form a switching system embodying an illustrative example of the invention, also shown in block diagram form; and FIG. 2 is a timing diagram for the operation of the system of FIG. 1.

Detailed Description

FIG. 1 illustrates the invention within the context of a communication switching system 10. As is conventional, system 10 comprises a plurality of switch-

ing stages 11 arranged in a switching matrix. An illustrative system of this type is the fast packet switching system disclosed in U.S. Patent No. 4,484,326.

Switching stages 11 are all the same. Each includes a switching element 12. For reliability purposes switching element 12 has been duplicated in this illustrative example. Each stage therefore includes two switching elements 12 and 13. Both elements 12 and 13 are normally active at the same time. The switching elements are conventional, each illustratively being a packet switching node such as is disclosed in the aforementioned patent.

Signal link 14, which carries input signals to a stage 11, is connected to the inputs of each element 12 and 13. In this illustrative example, stage input signal link 14 is an optical link carrying optical signals, whereas elements 12 and 13 are electrical signal-switching elements. Hence, link 14 is interfaced to the input of each element 12 and 13 by an optical-to-electrical signal converter 25. Such converters are well known in the art.

Each element 12 and 13 has two outputs. The outputs are treated identically—they are each connected to identical apparatus—and hence the connection of only one output will be discussed, with the understanding that the connection of the other output is the same.

First outputs of elements 12 and 13 are connected to element output links 15 and 16, respectively. In this illustrative example, links 15 and 16 also are optical links. Hence, they are interfaced to the outputs of the respective elements 12 and 13 by electrical-to-optical signal converters 26. Such converters are well-known in the art.

Each link 15 and 16 is connected to the input of a respective error-detection circuit 17 and 18, and to the input of a respective delay line 19 and 20. Error-detection circuits 17 and 18 may be any desired error-detection circuits. Many error detection schemes and circuits for implementing them are known in the art. For example, a parity error checker may be used to advantage for this purpose.

Links 15 and 16 are likely to be electrical links coupled directly to inputs of electrical circuits 17 and 18, and indirectly—via electrical-to-optical conversion circuits 26—to inputs of delay lines 19 and 20. However, for purposes of speed and reliability, it would be preferable to have circuits 17 and 18 be optical circuits. In such an arrangement, links 15 and 16 would be optical links, connected directly to the inputs of circuits 17 and 18. The latter, optical implementation is shown in FIG. 1. Should electrical circuits 17 and 18 be used in conjunction with optical links 15 and 16, the links would be coupled to the inputs thereof by means of optical-to-electrical conversion circuits such as circuits 25.

For reliability purposes, delay lines 19 and 20 are passive optical delay lines, such as lengths of optical

fiber. The delay of lines 19 and 20 is determined by the time needed to detect an error at circuits 17 and 18 and effect blocking of the errored signal at gates 21 and 22. For example, for links 15 and 16 operating at a data speed of 155 Mbps, using parity for error detection on 32 bit words, with a gate speed of approximately 0.01 usec, the delay is about 0.3 usec, or about 48m (150 feet) of optical fiber.

The outputs of delay lines 19 and 20 are connected to first inputs of optical AND gates 21 and 22, respectively. Second inputs of gates 21 and 22 are optically connected to outputs of error-detection circuits 17 and 18, respectively. The outputs of gates 21 and 22 are connected to inputs of an optical OR gate 23. The output of gate 23 is connected to a stage output signal link 24. Link 24 is an optical link like stage input signal link 14, and gates 21-23 are optical elements known in the art.

The operation of a switching stage 11, illustrated by the timing diagram of FIG. 2, is as follows. Signals—e.g., speech or data—in digital form are conducted by stage input signal link 14 to both switching nodes 12 and 13. Both nodes switch the incoming signals to one of their outputs—illustratively their first outputs—from whence the signals are conducted by element output links 15 and 16 to error-detection circuits 17 and 18 and delay lines 19 and 20, respectively. The outputs of nodes 12 and 13 are designated in FIG. 2 as input signal 1 and input signal 2, respectively. While the signals are passing through delay lines 19 and 20, error-detection circuits 17 and 18 process the received information to determine if an error therein has occurred, illustratively as a result of a malfunction in the switching elements 12 and 13, and generate signals indicative of the determination. The error signals generated by circuits 17 and 18 are designated in FIG. 2 as error signal 1 and error signal 2, respectively.

During the time that no error is found, both error-detection circuits 17 and 18 generate error signals enabling the associated gates 21 and 22 to pass-through signals received from the associated delay lines 19 and 20. The delayed signals output by delay lines 19 and 20 are designated in FIG. 2 as delayed signal 1 and delayed signal 2, respectively. When an error occurs, illustratively at point 200 in FIG. 2, it takes some time before its occurrence is detected. This time is designated as T 201 in FIG. 2. When the error is found, illustratively by error-detection circuit 17, it generates an output signal disabling the associated gate 21 from passing-through the received information, thereby causing the associated gate 21 to block the received information. The signals output by gates 21 and 22 are designated in FIG. 2 as output signal 1 and output signal 2, respectively. Delay lines 19 and 20 are sized to delay information input thereto for the operating time of circuits 17 and 18, so that the output signals of circuits 17 and 18 arrive at gates 21

and 22 either at the same time as or ahead of the information whose error status they represent. This delay time is designated in FIG. 2 as T 202.

The signal streams output by gates 21 and 22 are combined into a single signal stream by gate 23. If no error is detected by circuits 17 and 18, the signal streams output by gates 21 and 22 are identical, so the combined signal stream output by gate 23 is a duplicate of each of its component signal streams. If an error is detected by circuit 17 or 18, the corresponding signal stream is blocked by the associated gate 21 or 22, and the signal stream output by gate 23 is a duplicate of the remaining, error-free, signal stream input to gate 23. The signal output by gate 23 is designated in FIG. 2 as a combined output signal. When an error in the output of one of the switching elements 12 and 13 is detected and the corresponding signal stream is blocked, at no time is the signal stream output by switching stage 11 interrupted, lost, or otherwise corrupted thereby.

Of course, it should be understood that various changes and modifications to the illustrative embodiment described above will be apparent to those skilled in the art.

Claims

1. Apparatus for protecting a system against corruption or loss of output signal due to a malfunction, having a first and a second signal-handling component (12,13) for performing like signal-handling functions and adapted to receive a common input (14) signal, each component being for generating a separate output (15,16) signal from the common input signal, and CHARACTERISED BY malfunction detection means (17,18) connected to both of the components, for detecting occurrence of a malfunction affecting either of the output signals and generating a malfunction signal to indicate detection of the malfunction; signal-delay means (19,20) connected to the first and the second components for receiving the separate output signals, delaying the received signals while the malfunction-detection means are detecting occurrence of a malfunction affecting either of the received output signals that are being delayed, and outputting the received separate output signals after a delay of time sufficient for the malfunction-detection means to detect a malfunction and to generate the malfunction signal; and output means (21-23) connected to the signal delay means for receiving the delayed signals and outputting a system output (24) signal corresponding to at least one of the received delayed signals, the output means being responsive to the malfunction signal for outputting a signal corresponding only to a received de-



fiber. The delay of lines 19 and 20 is determined by the time needed to detect an error at circuits 17 and 18 and effect blocking of the errored signal at gates 21 and 22. For example, for links 15 and 16 operating at a data speed of 155 Mbps, using parity for error detection on 32 bit words, with a gate speed of approximately 0.01 usec, the delay is about 0.3 usec, or about 48m(150 feet) of optical fiber.

The outputs of delay lines 19 and 20 are connected to first inputs of optical AND gates 21 and 22, respectively. Second inputs of gates 21 and 22 are optically connected to outputs of error-detection circuits 17 and 18, respectively. The outputs of gates 21 and 22 are connected to inputs of an optical OR gate 23. The output of gate 23 is connected to a stage output signal link 24. Link 24 is an optical link like stage input signal link 14, and gates 21-23 are optical elements known in the art.

The operation of a switching stage 11, illustrated by the timing diagram of FIG. 2, is as follows. Signals--e.g., speech or data--in digital form are conducted by stage input signal link 14 to both switching nodes 12 and 13. Both nodes switch the incoming signals to one of their outputs--illustratively their first outputs--from whence the signals are conducted by element output links 15 and 16 to error-detection circuits 17 and 18 and delay lines 19 and 20, respectively. The outputs of nodes 12 and 13 are designated in FIG. 2 as input signal 1 and input signal 2, respectively. While the signals are passing through delay lines 19 and 20, error-detection circuits 17 and 18 process the received information to determine if an error therein has occurred, illustratively as a result of a malfunction in the switching elements 12 and 13, and generate signals indicative of the determination. The error signals generated by circuits 17 and 18 are designated in FIG. 2 as error signal 1 and error signal 2, respectively.

During the time that no error is found, both error-detection circuits 17 and 18 generate error signals enabling the associated gates 21 and 22 to pass-through signals received from the associated delay lines 19 and 20. The delayed signals output by delay lines 19 and 20 are designated in FIG. 2 as delayed signal 1 and delayed signal 2, respectively. When an error occurs, illustratively at point 200 in FIG. 2, it takes some time before its occurrence is detected. This time is designated as T 201 in FIG. 2. When the error is found, illustratively by error-detection circuit 17, it generates an output signal disabling the associated gate 21 from passing-through the received information, thereby causing the associated gate 21 to block the received information. The signals output by gates 21 and 22 are designated in FIG. 2 as output signal 1 and output signal 2, respectively. Delay lines 19 and 20 are sized to delay information input thereto for the operating time of circuits 17 and 18, so that the output signals of circuits 17 and 18 arrive at gates 21

and 22 either at the same time as or ahead of the information whose error status they represent. This delay time is designated in FIG. 2 as T 202.

The signal streams output by gates 21 and 22 are combined into a single signal stream by gate 23. If no error is detected by circuits 17 and 18, the signal streams output by gates 21 and 22 are identical, so the combined signal stream output by gate 23 is a duplicate of each of its component signal streams. If an error is detected by circuit 17 or 18, the corresponding signal stream is blocked by the associated gate 21 or 22, and the signal stream output by gate 23 is a duplicate of the remaining, error-free, signal stream input to gate 23. The signal output by gate 23 is designated in FIG. 2 as a combined output signal. When an error in the output of one of the switching elements 12 and 13 is detected and the corresponding signal stream is blocked, at no time is the signal stream output by switching stage 11 interrupted, lost, or otherwise corrupted thereby.

Of course, it should be understood that various changes and modifications to the illustrative embodiment described above will be apparent to those skilled in the art.

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layed signal which is unaffected by the malfunction.

2. Apparatus as claimed in claim 1 wherein the malfunction-detection means comprises means (17,18) for generating a first and a second malfunction signal (ERROR SIGNAL 1, ERROR SIGNAL 2) to indicate detection of a malfunction at the first and the second component, respectively, and the output means comprises means (21-23) responsive to the first and the second malfunction signals for transmitting at its output a signal corresponding only to the received delayed signal output by, respectively, the second and the first component.
3. Apparatus as claimed in claim 1 wherein the output means comprises signal-gating means (21,22) for receiving the delayed signals and transmitting a signal which includes at least one of the received delayed signals, the signal gating means being responsive to the malfunction signal for blocking the received delayed signal which is affected by the malfunction from being included in the signal transmitted by the signal-gating means.
4. Apparatus as claimed in claim 1 wherein the output means comprises means (21-23) for outputting a selected received delayed signal which is unaffected by the malfunction.
5. Apparatus as claimed in claim 1 wherein the output means comprises means (23) for combining the received delayed signals into a single signal and outputting the single signal, and means (21,22) responsive to the malfunction signal for blocking the received delayed signal which is affected by the malfunction from being combined into the single signal.
6. Apparatus as claimed in claim 1 wherein the signal delay means (19,20) operates separately from the malfunction detection means (17,18).
7. Apparatus as claimed in claim 1 wherein the first and the second signal-handling component (12,13) functionally duplicate each other and have a common signal input (14) and each has a separate signal output (15,16) for generating thereat an output signal from an input signal; the malfunction-detection means (17,18) detects malfunctions at the components at a point in the apparatus that precedes receipt of the output signals of the signal-handling components by the first and second signal-delay means and generates a first and a second signal (ERROR SIGNAL 1, ERROR SIGNAL 2) to indicate detection of

malfunction at the first and the second component, respectively; the output means comprises a first and a second signal-gating means (21,22) connected to the malfunction-detection means, each being for receiving the output signal generated by, respectively, the first and the second component, and for selectively transmitting the received signal, and each being respectively responsive to the first and the second malfunction signal for blocking the received output signal from being transmitted; the signal-delay means comprises a first and a second signal-delay means (19-20) connected to the output of, respectively, the first and the second signal-handling components to receive the output signal generated thereat, and connected, respectively, to the first and the second signal gating means to transmit the received output signal to the signal-gating means, each delay means being for delaying transmission of a received signal propagating therethrough for a period of time (T 202) sufficient for the connected gating means, when responding to a malfunction signal, to block those component output signals which are affected by the malfunction that is represented by the responded-to malfunction signal; and the output means further comprises output signal means (23) connected to the first and second signal-gating means to receive signals transmitted by the signal-gating means, for generating a signal corresponding to at least one of the received signals.

8. Apparatus as claimed in claim 7 wherein the output signal means comprises means (23) for combining signals received from the first and the second signal-gating means into the generated signal.
9. Apparatus as claimed in claim 7 wherein the output signal means comprises means (23) for selecting one of the signals received from the first and the second signal-gating means as the generated signal.
10. Apparatus as claimed in claim 7 wherein the malfunction-detection means comprises error-detection means (17,18) connected to the outputs of the signal-handling components for detecting errors in the output of either component.
11. Apparatus as claimed in claim 7 wherein the malfunction-detection means comprises fault-detection means (17,18) connected to the signal handling components for detecting faults in either component.
12. Apparatus as claimed in claim 7 wherein the signal-delay means are optical signal-delay means



(19,20), the signal-gating means are optical signal-gating means (21,22), and the signal-combining means are optical signal-combining means (23).

13. Apparatus as claimed in claim 12 wherein each optical signal-delay means (19,20) is a length of optical fiber, each signal-gating means is an optical AND gate (21,22), and the signal-combining means is either an optical OR gate (23) or an optical AND gate.

14. Apparatus as claimed in claim 7 wherein the signal-delay means (19,20), the signal-gating means (21,22), and the signal combining means (23) are passive devices.

15. Apparatus as claimed in claim 7 wherein each signal-handling component is a digital switching node (12,13).

16. Apparatus as claimed in claim 10 wherein the error-detection means comprises a first and a second error-detection circuit (17,18) each having an input connected to the output respectively of the first and second signal-handling component, for detecting errors in the output of the connected signal-handling component and generating a signal (ERROR SIGNAL 1, ERROR SIGNAL 2) to indicate detection of error.

17. A method of protecting a system against corruption or loss of output signal due to a malfunction, the system comprising a pair of components (12,13) having like signal-handling functions, both of which receive a common input (14) signal and each of which generates from the input signal a separate output (15,16) signal, comprising the steps of:

monitoring the system to detect (200) occurrence of a malfunction at either of the duplicated components;

generating a malfunction signal (ERROR SIGNAL 1) upon detection of a malfunction;

delaying (T 202) the output signals subsequently to the monitoring for a time sufficient to detect a malfunction and generate the malfunction signal (T 201);

generating a system output signal (COMBINED OUTPUT SIGNAL) corresponding to at least one of the delayed output signals; and

preventing generation of a system output signal corresponding to a delayed output signal affected by a malfunction (OUTPUT SIGNAL 1), in response to generation of the malfunction signal.

Patentansprüche

1. Vorrichtung zum Schutz eines Systems gegen eine Verfälschung oder den Verlust eines Ausgangssignals aufgrund einer Fehlfunktion mit einem ersten und einem zweiten Signalverarbeitungsbauteil (12,13), die gleiche Signalverarbeitungsfunktionen ausführen und ein gemeinsames Eingangssignal (14) aufnehmen, wobei jedes Bauteil ein getrenntes Ausgangssignal (15,16) aus dem gemeinsamen Eingangssignal erzeugt,

gekennzeichnet durch

eine an beide Bauteile angeschaltete Fehlfunktions-Detektoreinrichtung (17,18) zur Feststellung einer Fehlfunktion, die eines der Ausgangssignale beeinträchtigt, und zur Erzeugung eines Fehlfunktionssignals, das die Feststellung der Fehlfunktion anzeigt,

eine an das erste und das zweite Bauteil angeschaltete Signalverzögerungseinrichtung (19,20), die die getrennten Ausgangssignale empfängt, die empfangenen Signale verzögert, während die Fehlfunktions-Detektoreinrichtung das Auftreten einer Fehlfunktion feststellt, die eines der empfangenen und verzögerten Ausgangssignale beeinträchtigt, und die empfangenen, getrennten Ausgangssignale nach einer Verzögerungszeit ausgibt, die für die Fehlfunktions-Detektoreinrichtung ausreicht, eine Fehlfunktion festzustellen und das Fehlfunktionssignal zu erzeugen, und

eine an die Signalverzögerungseinrichtung angeschaltete Ausgangseinrichtung (21-23) zum Empfang der verzögerten Signale und zur Ausgabe eines Systemausgangssignals (24), das wenigstens einem der empfangenen, verzögerten Signale entspricht, wobei die Ausgangseinrichtung unter Ansprechen auf das Fehlfunktionssignal ein Signal ausgibt, das nur einem empfangenen, verzögerten Signal entspricht, das durch die Fehlfunktion unbeeinträchtigt ist.

2. Vorrichtung nach Anspruch 1, bei der die Fehlfunktions-Detektoreinrichtung eine Einrichtung (17,18) zur Erzeugung eines ersten und eines zweiten Fehlfunktionssignals (ERROR SIGNAL 1, ERROR SIGNAL 2), das die Feststellung einer Fehlfunktion beim ersten bzw. zweiten Bauteil anzeigt, und bei dem die Ausgangseinrichtung eine Einrichtung (21-23) umfaßt, die unter Ansprechen auf das erste und das zweite Fehlfunktionssignal an ihrem Ausgang ein Signal abgibt, das nur dem empfangenen, verzögerten Ausgangssignal des zweiten bzw. des ersten Bauteils entspricht.

3. Vorrichtung nach Anspruch 1, bei der die Aus-



gangseinrichtung eine Signalgattereinrichtung (21,22) umfaßt, die die verzögerten Signale aufnimmt und ein Signal überträgt, das wenigstens eines der aufgenommenen, verzögerten Signale enthält, wobei die Signalgattereinrichtung unter Ansprechen auf das Fehlfunktionssignal das empfangene, verzögerte und durch die Fehlfunktion beeinträchtigte Signal gegen eine Aufnahme in das durch die Signalgattereinrichtung übertragene Signal sperrt.

4. Vorrichtung nach Anspruch 1, bei der die Ausgangseinrichtung eine Einrichtung (21-23) zur Ausgabe eines gewählten, empfangenen und verzögerten Signale aufweist, das durch die Fehlfunktion ein unbeeinträchtigtes ist.

5. Vorrichtung nach Anspruch 1, bei der die Ausgangseinrichtung eine Einrichtung (23) zur Kombination der empfangenen, verzögerten Signale zu einem einzigen Signal und zur Ausgabe des einzigen Signals sowie eine Einrichtung (21,22) aufweist, die unter Ansprechen auf das Fehlfunktionssignal das empfangene, verzögerte und durch die Fehlfunktion beeinträchtigte Signal für eine Kombination zu dem einzigen Signal sperrt.

6. Vorrichtung nach Anspruch 1, bei der die Signalverzögerungseinrichtung (19,20) getrennt von der Fehlfunktions-Detektoreinrichtung (17,18) arbeitet.

7. Vorrichtung nach Anspruch 1, dadurch gekennzeichnet, daß das erste und das zweite Signalverarbeitungsbauteil (12,13) sich gegenseitig funktionell verdoppeln und einen gemeinsamen Signaleingang (14) sowie je einen getrennten Signalausgang (15,16) zur Erzeugung eines Ausgangssignals aus einem Eingangssignal aufweisen, daß die Fehlfunktions-Detektoreinrichtung (17,18) Fehlfunktionen bei den Bauteilen an einem Punkt in der Vorrichtung feststellt, der dem Empfang der Ausgangssignale der Signalverarbeitungsbauteile durch die erste und die zweite Verzögerungseinrichtung vorausgeht und ein erstes und ein zweites Signal (ERROR SIGNAL 1, ERROR SIGNAL 2) erzeugt, das die Feststellung einer Fehlfunktion beim ersten bzw. beim zweiten Bauteil anzeigt, daß die Ausgangseinrichtung eine erste und eine zweite, an die Fehlfunktions-Detektoreinrichtung angeschaltete Signalgattereinrichtung (21,22) umfaßt, die je das vom ersten bzw. zweiten Bauteil erzeugte Ausgangssignal aufnehmen und selektiv das aufgenommene Signal übertragen, und die je unter Ansprechen auf das erste bzw. zweite Fehlfunktionssignal eine Übertragung des

aufgenommenen Ausgangssignals sperren, daß die Signalverzögerungseinrichtung eine erste und eine zweite Signalverzögerungseinrichtung (19-20) umfaßt, die an den Ausgang des ersten bzw. zweiten Signalverarbeitungsbauteils angeschaltet sind und das dort erzeugte Ausgangssignal empfangen, und an die erste bzw. zweite Signalgattereinrichtung angeschaltet ist, um das empfangene Ausgangssignal zu der Signalgattereinrichtung zu übertragen, wobei jede Verzögerungseinrichtung die Übertragung eines empfangenen und durchlaufenden Signals um eine Zeitperiode (T_{202}) verzögert, die für die angeschaltete Gattereinrichtung beim Ansprechen auf ein Fehlfunktionssignal ausreicht, um diejenigen BauteilAusgangssignale zu sperren, die durch die Fehlfunktion beeinträchtigt sind, welche durch das jeweilige Fehlfunktionssignal dargestellt wird, und

daß die Ausgangseinrichtung ferner eine an die erste und zweite Signalgattereinrichtung angeschaltete Ausgangssignaleinrichtung (23) umfaßt, um von der Signalgattereinrichtung übertragene Signale zu empfangen und ein Signal zu erzeugen, das wenigstens einem der empfangenen Signale entspricht.

8. Vorrichtung nach Anspruch 7, bei der die Ausgangssignaleinrichtung eine Einrichtung (23) zur Kombination von Signalen aufweist, die von der ersten und der zweiten Signalgattereinrichtung empfangen worden sind, zu dem erzeugten Signal kombiniert.

9. Vorrichtung nach Anspruch 7, bei der die Ausgangssignaleinrichtung eine Einrichtung (23) umfaßt, die eines der von der ersten und der zweiten Signalgattereinrichtung empfangenen Signale als das erzeugte Signal auswählt.

10. Vorrichtung nach Anspruch 7, bei der die Fehlfunktions-Detektoreinrichtung eine Fehlerdetektoreinrichtung (17,18) umfaßt, die an den Ausgang der Signalverarbeitungsbauteile angeschaltet ist und Fehler im Ausgangssignal eines der Bauteile feststellt.

11. Vorrichtung nach Anspruch 7, bei der die Fehlfunktions-Detektoreinrichtung eine Fehlerdetektoreinrichtung (17,18) umfaßt, die an die Signalverarbeitungsbauteile angeschaltet ist und Fehler bei einem der Bauteile feststellt.

12. Vorrichtung nach Anspruch 7, bei der die Signalverzögerungseinrichtungen optische Signalverzögerungseinrichtungen (19,20), die Signalgattereinrichtungen optische Signalgattereinrichtungen (21,22) und die Signalkombiniereinrich-



tungen optische Signalkombiniereinrichtungen (23) sind.

13. Vorrichtung nach Anspruch 12, bei der jede optische Signalverzögerungseinrichtung (19,20) ein Stück einer optischen Faser ist, jede Signalgattereinrichtung ein optisches UND-Gatter (21,22) ist und die Signalkombiniereinrichtung entweder ein optisches ODER-Gatter (23) oder ein optisches UND-Gatter ist.

14. Vorrichtung nach Anspruch 7, bei der die Signalverzögerungseinrichtungen (19,20), die Signalgattereinrichtungen (21,22) und die Signalkombiniereinrichtungen (23) passive Bauteile sind.

15. Vorrichtung nach Anspruch 7, bei der jedes Signalverarbeitungsbauteil ein digitaler Vermittlungsknoten (12,13) ist.

16. Vorrichtung nach Anspruch 10, bei der die Fehlerdetektoreinrichtung eine erste und eine zweite Fehlerdetektorschaltung (17,18) umfaßt, die je mit einem Eingang an den Ausgang des ersten bzw. zweiten Signalverarbeitungsbauteils verbunden sind, um Fehler im Ausgangssignal des angeschalteten Signalverarbeitungsbauteils festzustellen und ein Signal (ERROR SIGNAL 1, ERROR SIGNAL 2) zu erzeugen, das die Feststellung eines Fehlers angibt.

17. Verfahren zum Schutz eines Systems gegen eine Verfälschung oder den Verlust eines Ausgangssignals aufgrund einer Fehlfunktion, wobei das System ein Paar von Bauteilen (12,13) mit gleichen Signalverarbeitungsfunktionen aufweist, die beide ein gemeinsames Eingangssignal (14) empfangen und je aus dem Eingangssignal ein getrenntes Ausgangssignal (15,16) erzeugen, mit den Verfahrensschritten:

Überwachen des Systems zur Feststellung (200) einer Fehlfunktion bei einem der verdoppelten Bauteile;

Erzeugen eines Fehlfunktionssignals (ERROR SIGNAL 1) bei Feststellung einer Fehlfunktion; Verzögern (T 202) der Ausgangssignale nach der Überwachung für eine ausreichende Zeit zur Feststellung einer Fehlfunktion und zur Erzeugung des Fehlfunktionssignals (T 201);

Erzeugen eines Systemausgangssignals (COMBINED OUTPUT SIGNAL), das wenigstens einem der verzögerten Ausgangssignale entspricht und Verhindern der Erzeugung eines Systemausgangssignals entsprechend einem verzögerten, durch eine Fehlfunktion beeinträchtigten Ausgangssignals (OUTPUT SIGNAL 1) unter Ansprechen auf die Erzeugung des Fehlfunktionssignals.

Revendications

1. Appareil pour protéger un système contre la corruption ou la perte d'un signal de sortie en raison d'une anomalie de fonctionnement, ayant un premier et un second composant de traitement de signaux (12,13) pour effectuer des fonctions de traitement de signaux semblables et adaptés pour recevoir un signal d'entrée commune (14), chaque composant servant à générer un signal de sortie séparée (15,16) à partir du signal d'entrée commune, et CARACTERISE PAR des moyens de détection d'anomalie de fonctionnement (17,18) connectés aux deux composants, pour détecter l'occurrence d'une anomalie de fonctionnement affectant l'un ou l'autre des signaux de sortie et générant un signal d'anomalie de fonctionnement pour indiquer la détection de l'anomalie de fonctionnement; des moyens de temporisation de signaux (19,20) connectés au premier et au second composant pour recevoir les signaux de sortie séparée, temporisant les signaux reçus pendant que les moyens de détection d'anomalie de fonctionnement détectent l'occurrence d'une anomalie de fonctionnement affectant l'un ou l'autre des signaux de sortie reçus qui sont temporisés, et sortant les signaux de sortie séparée reçus après une temporisation de temps suffisante pour que les moyens de détection d'anomalie de fonctionnement détectent une anomalie de fonctionnement et génèrent le signal d'anomalie de fonctionnement; et des moyens de sortie (21-23) connectés aux moyens de temporisation de signaux pour recevoir les signaux temporisés et sortir un signal de sortie de système (24) correspondant à au moins l'un des signaux temporisés reçus, le moyen de sortie étant sensible au signal d'anomalie de fonctionnement pour sortir un signal correspondant uniquement à un signal temporisé reçu qui n'est pas affecté par l'anomalie de fonctionnement.

2. Appareil selon la revendication 1, dans lequel le moyen de détection d'anomalie de fonctionnement comprend un moyen (17,18) pour générer un premier et un second signal d'anomalie de fonctionnement (SIGNAL D'ERREUR 1, SIGNAL D'ERREUR 2) pour indiquer la détection d'une anomalie de fonctionnement au premier et au second composant, respectivement, et le moyen de sortie comprend un moyen (21-23) sensible au premier et au second signal d'anomalie de fonctionnement pour transmettre à sa sortie un signal correspondant uniquement à la sortie du signal temporisé reçu par, respectivement, le second et le premier composant.

3. Appareil selon la revendication 1, dans lequel le



moyen de sortie comprend un moyen de transmission par porte de signaux (21,22) pour recevoir les signaux temporisés et transmettre un signal qui comporte au moins l'un des signaux temporisés reçus. le moyen de transmission par porte de signaux étant sensible au signal d'anomalie de fonctionnement pour empêcher le signal temporisé reçu qui est affecté par l'anomalie de fonctionnement d'être inclus dans le signal transmis par le moyen de transmission par porte de signaux.

4. Appareil selon la revendication 1, dans lequel le moyen de sortie comprend un moyen (21-23) pour sortir un signal temporisé reçu sélectionné qui n'est pas affecté par l'anomalie de fonctionnement.

5. Appareil selon la revendication 1, dans lequel le moyen de sortie comprend un moyen (23) pour combiner les signaux temporisés reçus en un signal unique et sortir le signal unique, et un moyen (21,22) sensible au signal d'anomalie de fonctionnement pour empêcher le signal temporisé reçu qui est affecté par l'anomalie de fonctionnement d'être combiné dans le signal unique.

6. Appareil selon la revendication 1, dans lequel le moyen de temporisation de signaux (19,20) fonctionne séparément du moyen de détection d'anomalie de fonctionnement (17,18).

7. Appareil selon la revendication 1, dans lequel le premier et le second composant de traitement de signaux (12,13) se doublent fonctionnellement l'un l'autre et ont une entrée de signal commune (14) et ont chacun une sortie de signal séparée (15,16) pour y générer un signal de sortie à partir d'un signal d'entrée; le moyen d'anomalie de fonctionnement (17,18) détecte les anomalies de fonctionnement aux composants à un point dans l'appareil qui précède la réception des signaux de sortie des composants de traitement de signaux par les premier et second moyens de temporisation de signaux et génère un premier et un second signal (SIGNAL D'ERREUR 1, SIGNAL D'ERREUR 2) pour indiquer la détection d'une anomalie de fonctionnement au premier et au second composant, respectivement; le moyen de sortie comprend un premier et un second moyen de transmission par porte de signaux (21,22) connectés au moyen de détection d'anomalie de fonctionnement, chacun servant à recevoir le signal de sortie généré par, respectivement, le premier et le second composant, et pour transmettre sélectivement le signal reçu, et chacun étant respectivement sensible au premier et au second signal d'anomalie de fonctionnement pour empê-

cher le signal de sortie reçu d'être transmis; le moyen de temporisation de signaux comprend un premier et un second moyen de temporisation de signaux (19-20) connectés à la sortie, respectivement, du premier et du second composant de traitement de signaux pour recevoir le signal de sortie qui y est généré, et connectés, respectivement, au premier et au second moyen de transmission par porte de signaux pour transmettre le signal de sortie reçu au moyen de transmission par porte de signaux, chaque moyen de temporisation servant à temporiser la transmission d'un signal reçu s'y propageant pendant une période de temps (T 202) suffisante pour que le moyen de transmission par porte connecté, alors sensible à un signal d'anomalie de fonctionnement, bloque les signaux de sortie des composants qui sont affectés par l'anomalie de fonctionnement qui est représentée par le signal d'anomalie de fonctionnement auquel il est répondu; et le moyen de sortie comprend en outre un moyen de signal de sortie (23) connecté au premier et au second moyen de transmission par porte de signaux pour recevoir des signaux transmis par le moyen de transmission par porte de signaux, pour générer un signal correspondant à au moins l'un des signaux reçus.

8. Appareil selon la revendication 7, dans lequel le moyen de signal de sortie comprend un moyen (23) pour combiner des signaux reçus du premier et du second moyen de transmission par porte de signaux dans le signal généré.

9. Appareil selon la revendication 7, dans lequel le moyen de signal de sortie comprend un moyen (23) pour sélectionner l'un des signaux reçus du premier et du second moyen de transmission par porte de signaux comme signal généré.

10. Appareil selon la revendication 7, dans lequel le moyen de détection d'anomalie de fonctionnement comprend un moyen de détection d'erreur (17,18) connecté aux sorties des composants de traitement de signaux pour détecter des erreurs dans la sortie de l'un ou l'autre composant.

11. Appareil selon la revendication 7, dans lequel le moyen de détection d'anomalie de fonctionnement comprend un moyen de détection d'erreur (17,18) connecté aux composants de traitement de signaux pour détecter des erreurs dans l'un ou l'autre composant.

12. Appareil selon la revendication 7, dans lequel les moyens de temporisation de signaux sont des moyens de temporisation de signaux optiques (19,20), les moyens de transmission par porte de



signaux sont des moyens de transmission par porte optiques (21,22), et les moyens de combinaison de signaux sont des moyens de combinaison de signaux optiques (23).

13. Appareil selon la revendication 12, dans lequel chaque moyen de temporisation de signaux optiques (19,20) est une longueur de fibre optique, chaque moyen de transmission par porte de signaux est une porte ET optique (21,22), et le moyen de combinaison de signaux est soit une porte OU optique (23) soit une porte ET optique.

14. Appareil selon la revendication 7, dans lequel les moyens de temporisation de signaux optiques (19,20), les moyens de transmission par porte de signaux (21,22), et les moyens de combinaison de signaux (23) sont des dispositifs passifs.

15. Appareil selon la revendication 7, dans lequel chaque composant de traitement de signaux est un noeud de commutation numérique (12,13).

16. Appareil selon la revendication 10, dans lequel le moyen de détection d'erreur comprend un premier et un second circuit de détection d'erreur (17,18) ayant chacun une entrée connectée à la sortie respectivement du premier et du second composant de traitement de signaux, pour détecter des erreurs dans la sortie du composant de traitement de signaux connecté et générer un signal (SIGNAL D'ERREUR 1, SIGNAL D'ERREUR 2) pour indiquer la détection d'une erreur.

17. Procédé de protection d'un système contre la corruption ou la perte d'un signal de sortie en raison d'une anomalie de fonctionnement, le système comprenant une paire de composants (12,13) ayant des fonctions de traitement de signaux semblables, recevant tous deux un signal d'entrée commune (14) et générant chacun à partir du signal d'entrée un signal de sortie séparée (15,16), comprenant les étapes de:

surveillance du système pour détecter (200) l'occurrence d'une anomalie de fonctionnement à l'un ou l'autre des composants doublés;

génération d'un signal d'anomalie de fonctionnement (SIGNAL D'ERREUR 1) à la détection d'une anomalie de fonctionnement;

temporisation (T 202) des signaux de sortie après la surveillance pendant une durée suffisante pour détecter une anomalie de fonctionnement et générer le signal d'anomalie de fonctionnement (T 201);

génération d'un signal de sortie (SIGNAL DE SORTIE COMBINE) correspondant à au moins l'un des signaux de sortie temporisés; et

interdiction de générer un signal de sortie du système correspondant à un signal de sortie temporisé affecté par une anomalie de fonctionnement (SIGNAL DE SORTIE 1), en réponse à la génération du signal d'anomalie de fonctionnement.

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