

ABSTRACT

A random walk method and apparatus (100) for parasitic capacitance extraction, and an electronic device (200) are provided. The method includes: taking a conductor most proximal to each boundary surface (23) of an integrated circuit layout as a boundary conductor (21); according to a Gaussian surface (22) corresponding to the boundary conductor (21), determining a first region and a second region; when a first hopping point is located in the second region, by taking the first hopping point as a center, constructing a first maximum transfer cube that does not intersect with any boundary surface (23), and randomly selecting a second hopping point on the first maximum transfer cube; and, when a second hopping point is located on a surface of any conductor or on any boundary surface (23), determining that a current random walk has been completed.

[FIG. 1]