A METHOD OF DIRECT BONDING TWO SUBSTRATES USED IN ELECTRONICS, OPTICS, OR OPTOELECTRONICS

The present invention relates to the field of fabricating a hybrid substrate for use in applications in electronics, optics, or optoelectronics.

More precisely, the invention relates to a method of "direct" bonding the two substrates, i.e. molecular bonding without any intermediate layer such as a layer of adhesive. The method can be implemented in a method of fabricating a hybrid substrate, as mentioned above.

In the state of the art, methods are already known for obtaining a hybrid substrate, which methods are based on a step of bonding a so-called "donor" substrate that includes the layer for transfer, onto a so-called "receiver" substrate, onto which said layer is to be transferred. Generally, an intermediate layer is interposed between them. The transfer is finished off by a step of removing a portion of the donor substrate known as the "remainder" in order to obtain said hybrid substrate in the end.

The hybrid substrate comprises in succession: the transferred layer, of thickness lying in the range 0.01 micrometers (μm) to a few μm; an intermediate layer of thickness lying typically in the range 0.01 μm to 1 μm; and the receiver substrate having thickness of several hundreds of μm.

The rear portion of the donor substrate can be removed by grinding and/or chemically etching the exposed face of the donor substrate, for example. Under such circumstances, it should be observed that the rear portion of the donor substrate is completely consumed.

Other techniques consist, prior to bonding, in forming a zone of weakness inside the donor substrate, then in removing the rear portion of the substrate by fracturing along said zone of weakness.

The zone of weakness may be obtained by implanting atomic species, such as hydrogen and/or rare gases, that technique being known under the trademark SMART CUT™.

The zone of weakness may also be obtained by a porous zone, by implementing the method known under the trademark ELTRAN™.

Reference can be made to the article "Silicon-on-insulator technology; materials to VLSI", 2nd edition by J.P. Colinge, published by Kluwer Academic Publishers, pp. 50 and 51, for more ample description of those techniques.

Those techniques of fabricating substrates are particularly well adapted and used for forming substrates of the type known under the term semiconductor-on-insulator (SeOI), with the best known form thereof being the silicon-on-insulator (SOI) substrate.

During the fabrication of such substrates, a layer of insulation is formed on the face of the donor substrate and/or the face of the receiver substrate for putting into intimate contact during the bonding step.

The insulator layer could be obtained by treating one of the substrates, e.g. by thermal oxidation, or indeed by depositing a layer of oxide. In the final substrate, the insulator layer is buried.

In all of those techniques for transferring layers, the quality of bonding has a direct impact on the final quality of the resulting substrate. In particular, the bonding energy with which the two substrates are bonded together during the subsequent step of removing the rear portion of the donor substrate is of particular importance.

It has been observed that the energy with which the two substrates are bonded together after being put into intimate contact is directly determined by the planeness of substrates, the possible presence of particles or contaminants on their surfaces, the roughness of said surfaces, or their degree of hydrophyly.

It has been found in the state of the art that an intermediate layer, referred to below as the "bonding layer", of thickness that is sufficient, i.e. greater than 50 nanometers (nm), when placed between two single-crystal substrates, serves to facilitate bonding by limiting the appearance of defects, e.g. blisters, at the contacting interface.

On this topic, reference can be made to the work by Q.Y. Tong and U. Gösele, "Semiconductor wafer bonding science and technology", published by John Wiley & Sons, New York (1999).

Thus, with a substrate of the SeOI type, the buried insulating layer serves to facilitate and limit bonding defects.

Unfortunately, there exist situations in which it is preferable to limit the thickness of this buried insulating layer to values of less than about 50 nm, or even to eliminate it completely, in order to transfer the working layer of the donor substrate directly onto the receiver substrate.

This applies for example when it is desired to optimize heat conduction between the receiver substrate and the transferred layer in which the microelectronic components are to be formed, for the purpose of dumping a maximum amount of the heat generated by the components while they are in use.

Bonding without a buried insulating layer also serves to improve electrical conduction between the transferred layer and the receiver substrate, and at least to obtain contact that is electrically conductive.

It can also be desirable to combine a transferred layer and a receiver substrate presenting respective crystal orientations that are different, e.g. in order to optimize the performance of transistors made respectively in both of these portions of the hybrid substrate.

By way of example, for components of the complementary metal oxide semiconductor (CMOS) type, it

can be envisaged to make the NMOS transistor on the transferred layer or on the receiver layer made out of (100) oriented silicon, and the PMOS transistor respectively on the receiver substrate or the transferred layer, made out of (110) oriented silicon.

The following articles: K.L. Saenger et al. "Amorphization/templated recrystallization method for changing the orientation of single-crystal silicon: an alternative approach to hybrid orientation substrates", Appl. Phys. Lett., 87, 221911 (2005), and C.Y. Sung et al. "High performance CMOS bulk technology using direct silicon bond (DSB) mixed crystal orientation substrates", Tech. Dig. - Int. Electron Devices Meet., 2005, 236, set out the different electrical characteristics of silicon depending on its crystal orientation.

It can also be useful to make hybrid substrates comprising a receiver substrate of solid silicon covered in a transferred layer of silicon or of germanium or of silicon-germanium that is elastically stressed in tension or in compression.

Bonding techniques already exist. Nevertheless, it is difficult to implement them industrially in terms of the quality required for an application to transferring layers, when the bonding is so-called "direct" bonding, i.e. without any additional intermediate bonding layer, or when the techniques involved use a bonding layer of thickness that is limited, being less than about 50 nm.

On this topic, reference can be made to the article by S.L. Holl et al., "UV activation treatment for hydrophobic wafer bonding", Journal of the Electrochemical Society, 153 (7), G613 - G616 (2006) which shows the difficulties in obtaining defect-free bonding.

Those prior art techniques are hydrophilic bonding and hydrophobic bonding.

By way of example, hydrophilic bonding of silicon-on-silicon consists in performing hydrophilic cleaning of

the substrates prior to putting them into intimate contact.

Such cleaning is typically performed by a method known as the "RCA" method which consists in treating the surfaces for bonding in succession with:

· a first bath of a solution known as Standard Clean 1 (SC1) and that comprises a mixture of ammonium hydroxide (NH_4OH), of hydrogen peroxide (H_2O_2), and of deionized water; and then

· a second bath of a solution known as Standard Clean 2 (SC2) that comprises a mixture of hydrochloric acid (HCl), of hydrogen peroxide (H_2O_2), and of deionized water.

On this topic, it is also possible to read the article by C. Maleville, O. Rayssac, H. Moriceau et al., in Proc. 4th Internat. Symposium on Semiconductor Wafer Bonding: PV 97-36, ECS publications, p. 46, 1997.

Hydrophobic bonding is usually implemented by cleaning the surfaces in a bath of hydrofluoric acid (HF) prior to putting them into contact, said cleaning being known to the person skilled in the art as "HF last" cleaning. Such a cleaning method is typically followed by specific rinsing and drying steps, which make the procedure rather complex. In addition, the surfaces as treated in that way are very reactive to metallic contaminants and to particles, which means that special precautions must be taken. It is therefore not easy to industrialize that technique.

Other hydrophobic bonding methods exist, such as cleaning in hydrofluoric acid (HF) vapor, or annealing in an ultra-high vacuum (UHV). On this topic, reference can be made to the article by M.J. Kim and R.W. Carpenter, "Heterogeneous silicon integration by ultra-high vacuum wafer bonding", Journal of Electrochemical Materials, Vol. 32, No. 8, 2003.

One of the main limitations of the above-mentioned methods is the difficulty in implementing them, which

applies in particular for ultra-high vacuum annealing, which requires the use of equipment that is expensive.

Furthermore, the above-mentioned hydrophilic and hydrophobic bonding methods are generally followed by thermal annealing in the range 200°C to 1200°C for a few hours (h), e.g. for 2 h. Unfortunately, after annealing in the range 200°C to 1100°C, bubbles have been observed in the bonding interface using an infrared transmission technique. Such degassing is probably due to desorbing of the species present at the bonding interface, regardless of whether the bonding is hydrophilic or hydrophobic.

Furthermore, after annealing in the range 1100°C to 1200°C, these bubbles are not necessarily any longer observable by infrared transmission. Nevertheless, this absence of visible bubbles does not mean that the bonding is perfect, i.e. that it presents high bonding energy. On this topic, reference can be made for example to the article by R.D. Horning and R.R. Martin, "Wafer-to-wafer bond characterization by defect decoration etching", Second International Symposium on Semiconductor Wafer Bonding: Science Technology and Applications, PV 93-29, pp. 199, 1993.

Sometimes, it is even possible to observe defects after annealing above 1100°C, by using the acoustic microscopy technique.

It is possible to cure these bonding defects or to prevent them from appearing by heat treatment at a temperature that is greater than or equal to 1100°C. Nevertheless, depending on the intended subsequent applications, it is not always possible to envisage applying heat treatment at such a high temperature. It can sometimes even be desirable not to exceed 200°C.

Methods enabling the defects observed during direct bonding are described in the literature. They consist in creating trenches or performing desorption on surfaces prior to bonding. Nevertheless, those methods are not

entirely satisfactory as mentioned in the article by R.H. Esser, K.D. Hobart, and F.J. Kub, "Improved low temperature Si-Si hydrophilic wafer bonding", Journal of the Electrochemical Society, 150(3), G228-G231 (2003). In addition, such substrates with trenches are not always suitable for use in certain applications for fabricating electronic components.

Embodiments of the present invention seek to remedy the above-mentioned drawbacks of the prior art.

In particular, embodiments of the present invention seek to provide a method enabling two substrates to be bonded directly one against the other without any additional bonding layer, at least one of the substrates comprising a layer semiconductor material on one of its face or in the proximity thereof, and for this to be done with quality that is satisfactory and without macroscopic bonding defects such as bubbles appearing.

In accordance with a first aspect of the present invention, there is provided a method of direct bonding of so-called "front" faces of two substrates for use in applications in the fields of electronics, optics, or optoelectronics, at least one of the two substrates referred to as the "substrate comprising a semiconductor" comprising a layer of semiconductor material that extends over its front face or in the proximity thereof,

said method being characterized in that it comprises the following steps consisting in:

· subjecting at least the front face of the substrate that comprises a semiconductor, or at least one of the front faces of both substrates if both substrates comprise a semiconductor, to heat treatment referred to as "preparation treatment prior to bonding", at a temperature lying in the range 900°C to 1200°C, in a gaseous atmosphere comprising hydrogen and/or argon, for a duration of at least 30 seconds (s); and

· bonding directly together said respective front faces of the two substrates for bonding together.

The method according to embodiments of the present invention can make it possible to eliminate the native oxide present on the treated surface and also make it possible to passivate said surface by means of hydrogen atoms.

Contrary to the state of the art, the method can be used with good results, even if the substrates do not have an insulating layer, or if they do have an insulating layer but with a thickness of less than about 50 nm.

In addition, the preparation treatment prior to bonding can make it possible to obtain very low levels of roughness. It has been possible to measure root mean square (rms) roughness of 0.7 angstroms (Å) on a scanned 2 µm by 2 µm sample, whereas the surface of a silicon substrate typically presents rms roughness of the order of 2 Å and the usual surface preparation treatments prior to bonding (such as SC1 type cleaning) tend to make the surface even rougher.

Embodiments of the invention thus can present the additional advantage of putting into contact surfaces that present very little roughness.

According to embodiments of the invention that are advantageous and non-limiting, taken singly or in combination:

· said preparation treatment prior to bonding is performed in a gaseous atmosphere containing argon exclusively or containing hydrogen exclusively;

· said preparation treatment prior to bonding is performed in a rapid thermal annealing (RTA) type chamber or in a conventional chamber or within a chamber of an epitaxy plant;

· the direct bonding is performed immediately after said preparation treatment prior to bonding;

· the substrate(s) subjected to said preparation treatment prior to bonding is/are stored temporarily in a chamber under a controlled inert gas atmosphere prior to said direct bonding;

· after said direct bonding, bonding consolidation heat treatment is performed at a temperature lying in the range 200°C to 1200°C, for about at least one hour, preferably for less than three hours;

· both substrates for bonding comprise a semiconductor, and the front faces of the both substrates are subjected to the preparation treatment prior to bonding; and

· said semiconductor material is selected from (100) silicon, (110) silicon, and (111) silicon.

In accordance with a second aspect of the present invention, there is provided a method of fabricating a hybrid substrate suitable for being used in applications in the fields of electronics, optics, or optoelectronics, the method being characterized in that it comprises the following steps consisting in:

· selecting a so-called "receiver" substrate having one of its faces referred to as a "front" face;

· selecting a so-called "donor" substrate that comprises a layer of material for transfer, and another portion referred to as its "remainder", said layer for transfer extending over one of the faces of the donor substrate, referred to as its "front" face;

at least one of said receiver and donor substrates comprising a layer of semiconductor material extending over its front face or in the proximity thereof;

· proceeding with direct bonding of the two respective front faces of the donor substrate and of the receiver substrate in accordance with the above-specified method; and

· removing the remainder from said donor substrate in order to obtain said hybrid substrate comprising the receiver substrate and the transferred layer.

According to embodiments of the present invention that are advantageous, taken singly or in combination:

· at least one of the donor and receiver substrates comprises a layer of insulating material on said layer of

semiconductor material, and said layer of insulating material extends over the front face of said substrate;

· said layer of insulating material presents thickness that is less than or equal to 50 nm;

· said layer of insulating material is a layer of native oxide;

· the remainder of the donor substrate is removed by mechanical and/or chemical thinning;

· prior to the direct bonding, a zone of weakness is formed inside the donor substrate, and at least a portion of the remainder of the donor substrate is removed along said zone of weakness by applying mechanical, chemical, and/or thermal stresses;

· the zone of weakness is formed by implanting atomic species, the receiver substrate comprises a layer of semiconductor material, and only the receiver substrate is subjected to the preparation treatment prior to bonding; and

· the zone of weakness is a porous zone.

Other characteristics and advantages of the invention appear from the following description given with reference to the accompanying drawings which show one possible implementation by way of non-limiting indication.

In the drawings:

· Figures 1A to 1C show the various steps of a method of fabricating a hybrid substrate, implementing the direct bonding method in accordance with the invention; and

· Figures 2A to 2C, 3A to 3D, and 4A to 4C show respectively three variant implementations of the above method.

The invention relates to a method of directly bonding a donor substrate on a receiver substrate.

In the figures, the receiver substrate is given reference 1. It presents a so-called "front" face 11

that is to come into contact with the donor substrate 2, and a so-called "rear" face 12 that is opposite.

Similarly, the receiver substrate 2 presents a front face 21 and a rear face 22.

The donor substrate 2 and the receiver substrate 1 may be single-layer or multilayer substrates.

At least one of the donor and receiver substrates 2 and 1 comprises a layer of semiconductor material.

In other words, one of them can be made out of a material that is not a semiconductor material, for example an insulator material, such as sapphire or an oxidized substrate.

The term "at least one of them comprises a layer of semiconductor material" means that one of the two substrates 1 or 2, or both of them is/are made of semiconductor material, either completely for a single-layer substrate, or at least in part for a multilayer substrate.

For a multilayer substrate, the layer of semiconductor material extends along the front face of the substrate (see for example Figure 2A) or in the proximity thereof (see for example Figure 4A). The term in the "proximity" of means that the layer of semiconductor material may be covered in a third layer of insulation, e.g. of oxide, having a thickness of less than about 10 nm, or even in a very fine layer of insulation presenting thickness that is of the order of a few Å (1 nm = 10 Å), e.g. a native oxide layer.

In similar manner, the single-layer substrate of semiconductor material may also be covered by a layer of insulation as described in the above paragraph.

The semiconductor materials are those that are generally frequently used in the field of microelectronics, namely, for example (100) silicon, (110) silicon, or (111) silicon, where the numerical references specify crystallographic types.

The invention consists in subjecting at least one of the faces for bonding, i.e. at least one of the front faces 11 and/or 21, to heat treatment at a temperature lying in the range 900°C to 1200°C, in a gaseous atmosphere comprising hydrogen and/or argon, but no oxygen.

When both substrates comprise a semiconductor material, then this treatment is preferably performed on each of their front faces.

The gaseous atmosphere may thus be selected to comprise: exclusively hydrogen, or exclusively argon, or a mixture of both of them, or even one or other of them associated with some other gas, excluding oxygen.

The duration of the treatment is at least 30 s, and preferably does not exceed a few minutes (min).

The effect of hydrogen and/or argon is to eliminate any native oxide that might be present on the treated front face(s) and to passivate said surface(s) with hydrogen atoms. It also serves to obtain surface roughnesses that are very small.

This preparation treatment prior to bonding also has the effect of making the bonded surfaces hydrophobic. This has been demonstrated by measuring the contact angle of a drop of water, which gave a value of 80°. This value is considerably greater than the value that is obtained after treatment of the "HF last" type, which is typically 70°, see the article by Y. Bäcklünd, Karin Hermasson, L. Smith, "Bond-strength measurements related to silicon surface hydrophilicity", J. Electrochem. Soc., Vol. 1398, No. 8, 1992.

The advantage of the method in accordance with the invention is that no species is adsorbed on the surface. Since hydrogen atoms are very small, on being desorbed to create covalent bonds between the facing front faces 11 and 12, they do not remain trapped at the interface, but diffuse into the material, and thus do not generate a degassing defect.

In addition, since the method in accordance with the invention involves dry treatment, unlike the above-mentioned "HF last" treatment, for example, it is simpler to implement since it does not require drying.

The method in accordance with the invention can be implemented in a chamber that enables high temperature annealing to be performed under a controlled atmosphere, e.g. a single-plate rapid thermal annealing (RTA) type chamber, or indeed a chamber of an epitaxy plant.

It is also possible to envisage using a traditional chamber in which the substrates are processed in batches.

After the above-mentioned surface treatment, bonding must be performed very quickly in order to minimize any risk of the treated front faces being contaminated by the ambient atmosphere. This bonding step is shown in Figures 1B, 2B, 3B, and 4B.

The bonding interface is given reference 3.

Advantageously, it is also possible to store the treated substrates in a chamber in which the atmosphere is controlled so as to contain an inert gas only, typically argon or nitrogen. Such treatment makes it possible to lengthen waiting time before the donor and receiver substrates 2 and 1 are bonded together.

It has also been observed that surfaces prepared in application of the method of the invention are much less reactive than are surfaces prepared by the above-mentioned "HF last" method, thereby limiting particle contamination of such surfaces. This makes industrialization easier.

Advantageously, after bonding, it is also possible to proceed with pre-consolidation or consolidation heat treatment at a temperature lying in the range 200°C to 1200°C, preferably in the vicinity of at least 1100°C if it is desired to consolidate the interface entirely.

This treatment preferably lasts for at least one hour and preferably for less than three hours, so as to reinforce bonding. This pre-consolidation or

consolidation steps takes place without bubbles forming, thereby ensuring good bonding energy at all locations of the wafer.

The direct bonding method can be implemented in a method of fabricating a hybrid substrate.

The method of fabricating a hybrid substrate comprises the following steps consisting in:

· selecting a donor substrate 2 and a receiver substrate 1 of the above-specified type;

· performing the surface temperature and bonding steps in accordance with the above-described direct bonding method; and

· removing a portion of the donor substrate so as to obtain a hybrid substrate that comprises the receiver substrate 1 having the transferred layer taken from the donor substrate bonded thereto.

With reference to Figures 1A to 1C, there can be seen an example of preparing a hybrid substrate 4 from donor and receiver substrates 2 and 1, both of which are single-layer substrates.

After surface treatment in accordance with the invention and bonding, a portion of the donor substrate referred to as the "remainder" is removed by mechanical thinning of the abrading and polishing type so as to obtain the transferred layer 20.

Figures 2A to 2C show a variant implementation in which the donor substrate 2 includes a zone of weakness 25.

In this example, the zone of weakness 25 is obtained by implanting atomic species, e.g. hydrogen ions, using the method known under the name SMART CUT™. The zone of weakness 25 defines a layer 23 for transferring from the remainder 24 of the source substrate 2.

Under such circumstances, it should be observed that the donor substrate cannot subsequently be subjected to the above-described preparation treatment prior to bonding. The heat treatment of the invention would run

the risk of causing bubbles to be formed at a front face 21. Only the receiver substrate 1 is subjected to such treatment.

The substrate 1 comprises a layer 13 of semiconductor material, e.g. of silicon, and on its surface it may include a fine layer of native oxide.

The source substrate 2 may optionally be treated using the above-mentioned "HF last" method, or some other technique enabling a hydrophobic or hydrophilic surface to be obtained. The source substrate may include a non-semiconductive layer (13) on its front face.

In a variant implementation that is not shown in the figures, this zone of weakness 25 could also be a porous layer, e.g. obtained using the method known under the trademark ELTRAN.

After the surface treatment and the direct bonding of the two substrates 1 and 2, the remainder 24 of the donor substrate 2 is removed by applying stresses of mechanical, chemical, and/or thermal type, in accordance with the techniques commonly used in implementing the SMART CUT™ method.

The hybrid substrate 5 is obtained as shown in Figure 2 which comprises layers 13 and 23 of semiconductor material and a layer 14 of the donor substrate 1.

Figures 3A to 3C show another embodiment of a hybrid substrate in accordance with the invention, when the donor substrate 2 is a substrate of the semiconductor-on-insulation type. The receiver substrate 1 is identical to that described in Figure 1A.

The donor substrate 2 comprises two layers of semiconductor material 26 and 272, together with an insulating layer 271.

After the bonding step shown in Figure 3B, the remainder 27 is removed in two stages.

A first step shown in Figure 3C consists in mechanically removing the layer 272, by abrading and then polishing.

The second step consists in removing the layer of insulation 271, e.g. by chemical etching.

The substrate as finally obtained comprises the receiver substrate 1 having the transferred layer 26 bonded thereto and given overall reference 6.

The various techniques for removing the remainder of the source substrate 2 as described above can also be used in combination, depending on the nature of the donor substrate 2.

Finally, a fourth variant implementation of the invention is described below with reference to Figures 4A to 4C.

The receiver substrate 1 is a single layer, and it is not a semiconductor.

The donor substrate 2 is similar to that of Figure 2A, and it is not covered in an insulating layer 28.

After preparation treatment prior to bonding in accordance with the invention, after the bonding step (and possibly also consolidation step) as described above and shown in Figure 4B, and after the remainder 24 has been removed, the hybrid substrate 7 is obtained.

The hybrid substrate 7 comprises the receiver substrate 1 and the transferred insulator and semiconductor layers 28 and 23.

Five examples of making a silicon-silicon hybrid substrate are described below.

Example 1, showing the principle

The source substrate 2 and the receiver substrate 1 were silicon substrates having the (100) crystal orientation and a diameter of 300 millimeters (mm).

Both substrates 1 and 2 were subjected to heat treatment at a temperature of 1060°C for a duration of 3 min in an atmosphere containing 100% hydrogen.

The treatment was performed in an epitaxy plant. Beforehand, the substrates were cleaned using baths of ozone + SC1 solution, and then rinsed in deionized water.

The number of additional particles was measured by a laser surface scanner device of the kind sold under the trademark Surfscan SP1, by the supplier KLA-Tencor. The measurements were performed before the surface treatment and then after bonding. It was found that the treatment in accordance with the invention led to fewer than 50 particles with a size of 0.13 µm or more being added.

The respective front faces of the donor substrate and of the receiver substrate were then subjected to direct bonding.

The resulting stack was subjected to consolidated heat treatment at a temperature close to 1100°C for 2 h.

The quality of the bonding was measured by acoustic microscopy: no bonding defect was detected.

Example 1 for comparison

Silicon wafers (substrates) were prepared by cleaning similar to that performed in Example 1, and then subjected to "HF last" treatment.

Prior to bonding, the number of additional particles having a size of 0.13 µm or greater was counted and found to be more than 800.

After bonding and consolidation annealing at 1100°C for 2 h, bonding defects could be observed by using acoustic microscopy.

The method in accordance with the invention is thus more effective, see Example 1.

Example 2: analysis of hydrophobic bonding after various types of pre-consolidation or consolidation thermal annealing

The procedure was the same as in Example 1, but the bonding step was followed by various different thermal annealing steps as listed below:

a) annealing temperature: 200°C; duration 2 h;

b) annealing temperature/duration: 350°C for 2 h, followed by a rise to 500°C at a rate of 5°C/min, followed by a plateau at 500°C for 1 h;

c) annealing temperature/duration: same anneal as in b) but with a rise to a plateau at 700°C; and

d) annealing temperature/duration: same anneal as in b) but with a rise to a plateau at 900°C.

After bonding, respectively before the annealing heat treatment and after it, the substrates were observed using an acoustic microscopic.

None of them presented any bubbles.

Furthermore, substrates were prepared by annealing in an RTA type chamber at 1100°C for 60 s in an atmosphere containing 20% hydrogen and 80% oxygen, after which they were bonded and subjected to the same consolidation anneals.

The same good results were observed, i.e. no bonding defects such as bubbles.

Example 3

This example corresponds to a variant of the above example, in which the donor substrate 2 was an SOI type substrate with its silicon surface layer constituting the layer for transfer. The silicon layer and the silicon oxide layer were removed respectively by polishing and tetramethylammonium hydroxide (TMAH), and by chemical etching using hydrofluoric acid (HF). A receiver substrate 1 was obtained covered in a transferred layer of silicon.

The tests were repeated, and followed by the various pre-consolidation or consolidation treatments mentioned in Example 2.

The hybrid substrates that were obtained did not present any bubbles.

Example 4

This example constitutes a variant of Example 1, in which the source substrate was subjected to implantation of atomic species, in order to form a zone of weakness therein.

In this context, the source substrate can be oxidized prior to the implantation step. The oxide layer can be constituted by a native oxide having a thickness of a few nanometers or it can be formed voluntarily and reach a thickness close to 50 nm.

The implantation consisted in implanting hydrogen ions at a density of $5\times10^{16}H^2/cm^2$, with an energy of 60 kiloelectron volts (keV), so as to locate the hydrogen concentration peak in the zone of weakness which was constituted by buried defects.

As explained above, the donor substrate need not be subjected to treatment in accordance with the invention. It can be subjected to conventional hydrophilic or hydrophobic surface treatment, for example treatment of the above-described RCA type.

The silicon receiver substrate was subjected to treatment in accordance with the invention.

The donor and receiver substrates were then put into contact via their respective front faces, and they were then subjected to pre-consolidation treatment at 200°C.

The remainder of the source substrate was detached by applying thermal stresses, i.e. treatment at a temperature of about 400°C to about 600°C for a duration of 2 h to 8 h, or by applying mechanical stresses.

The final substrate was advantageously then subjected to a finishing step since its free surface becomes slightly damaged during detachment along the zone of weakness. The finishing step can be performed by

smoothing heat treatment, by sacrificial oxidation, and/or by polishing.

No bubbles were observed at the bonding interface.

In order to improve the mechanical strength of the bonding, an additional step could be provided of plasma activation on one or both faces for being put into contact.

CLAIMS

1. A method of direct bonding of so-called "front" faces of two substrates for use in applications in the fields of electronics, optics, or optoelectronics, at least one of the two substrates referred to as the "substrate comprising a semiconductor" comprising a layer of semiconductor material that extends over its front face or in the proximity thereof, said method being characterized in that it comprises the following steps consisting in:

· subjecting at least the front face of the substrate that comprises a semiconductor, or at least one of the front faces of both substrates if both substrates comprise a semiconductor, to heat treatment referred to as "preparation treatment prior to bonding", at a temperature lying in the range 900°C to 1200°C, in a gaseous atmosphere comprising hydrogen and/or argon, for a duration of at least 30 s; and

· bonding directly together said respective front faces of the two substrates for bonding together.

2. A method according to claim 1, characterized in that said preparation treatment prior to bonding is performed in a gaseous atmosphere containing argon exclusively.

3. A method according to claim 1, characterized in that said preparation treatment prior to bonding is performed in a gaseous atmosphere containing hydrogen exclusively.

4. A method according to any preceding claim, characterized in that said preparation treatment prior to bonding is performed in a rapid thermal annealing (RTA) type chamber.

5. A method according to any one of claims 1 to 3, characterized in that said preparation treatment prior to bonding is performed in a traditional heat treatment chamber.

6. A method according to any one of claims 1 to 3, characterized in that said preparation treatment prior to bonding is performed in a chamber of an epitaxy plant.

7. A method according to any preceding claim, characterized in that the direct bonding is performed immediately after said preparation treatment prior to bonding.

8. A method according to any one of claims 1 to 6, characterized in that the substrate(s) subjected to said preparation treatment prior to bonding is/are stored temporarily in a chamber under a controlled inert gas atmosphere prior to said direct bonding.

9. A method according to any preceding claim, characterized in that after said direct bonding, bonding consolidation heat treatment is performed at a temperature lying in the range 200°C to 1200°C, for about at least one hour.

10. A method according to any preceding claim, characterized in that after said direct bonding, bonding consolation heat treatment is performed at a treatment lying in the range 200°C to 1200°C for less than three hours.

11. A method according to any preceding claim, characterized in that both substrates for bonding comprise a semiconductor, and in that the front faces of the both substrates are subjected to the preparation treatment prior to bonding.

12. A method according to any preceding claim, characterized in that said semiconductor material is selected from (100) silicon, (110) silicon, and (111) silicon.

13. A method of fabricating a hybrid substrate suitable for being used in applications in the fields of electronics, optics, or optoelectronics, the method being characterized in that it comprises the following steps consisting in:

· selecting a so-called "receiver" substrate having one of its faces referred to as a "front" face;

· selecting a so-called "donor" substrate that comprises a layer of material for transfer, and another portion referred to as its "remainder", said layer for transfer extending over one of the faces of the donor substrate, referred to as its "front" face;

at least one of said receiver and donor substrates comprising a layer of semiconductor material extending over its front face or in the proximity thereof;

· proceeding with direct bonding of the two respective front faces of the donor substrate and of the receiver substrate in accordance with the method according to any preceding claim; and

· removing the remainder from said donor substrate in order to obtain said hybrid substrate comprising the receiver substrate and the transferred layer.

14. A method according to claim 13, characterized in that at least one of the donor and receiver substrates comprises a layer of insulating material on said layer of semiconductor material,

and in that said layer of insulating material extends over the front face of said substrate.

15. A method according to claim 14, characterized in that said layer of insulating material presents thickness that is less than or equal to 50 nm.

16. A method according to claim 14 or claim 15, characterized in that said layer of insulating material is a layer of native oxide.

17. A method according to any one of claims 13 to 16, characterized in that the remainder of the donor substrate is removed by mechanical and/or chemical thinning.

18. A method according to any one of claims 13 to 17, characterized in that prior to the direct bonding, a zone of weakness is formed inside the donor substrate, and in that at least a portion of the remainder of the donor substrate is removed along said zone of weakness by applying mechanical, chemical, and/or thermal stresses.

19. A method according to claim 18, characterized in that the zone of weakness is formed by implanting atomic species, in that the receiver substrate comprises a layer of semiconductor material, and in that only the receiver substrate is subjected to the preparation treatment prior to bonding.

20. A method according to claim 18, characterized in that the zone of weakness is a porous zone.