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ABSTRACT

A NEW METHOD FOR PRE-STI-CMP PLANARIZATION USING POLY-SI THERMAL OXIDATION

A method of forming shallow trench isolations is described. An etch stop layer is deposited on the surface of a semiconductor substrate. A plurality of isolation trenches are etched through the etch stop layer into the semiconductor substrate to separate active areas. An oxide layer is deposited over the etch stop layer and within the isolation trenches wherein the oxide fills the isolation trenches and overlies the etch stop layer on the active areas. A polysilicon layer is deposited overlying the oxide layer within the isolation trenches and the oxide layer overlying the etch stop layer. The polysilicon layer is polished away until the oxide layer overlying the etch stop layer is exposed and the polysilicon layer remains only overlying the oxide layer in the isolation trenches. The polysilicon layer is oxidized whereby the oxidized polysilicon layer has a height close to the height of the oxide layer overlying the etch stop layer. The oxidized polysilicon layer, the oxide layer overlying the etch stop layer, and the oxide layer in the isolation trenches is polished down until the etch stop layer is reached thereby planarizing the isolation trenches to complete planarized shallow trench isolation regions in the manufacture of an integrated circuit device.

FIGURE 6

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