

SPECIFICATION

A monolithic semiconductor integrated circuit for television receivers

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The present invention relates to a monolithic semiconductor integrated circuit for television receivers.

10 A signal processing circuit formed in a monolithic semiconductor integrated circuit for television receivers is known, for example, in IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. SC-4, No. 4, pp.202-210, published in August, 1969.

15 On the other side of the monolithic semiconductor integrated circuit it is known to provide a tuner, a video intermediate-frequency amplifier, and a video detector. The video intermediate-frequency output signals
20 obtained from the tuner are amplified by the video intermediate-frequency amplifier, and the output of the video intermediate-frequency amplifier is applied to the input of the video detector. The detected signals produced by
25 the video detector are fed to the input of a video amplifier in the monolithic semiconductor integrated circuit. The video output signals of the video amplifier in the integrated circuit are fed to the input of a synchronous separator
30 in the integrated circuit. The outputs of the synchronous separator are fed to a vertical oscillation output circuit and to a horizontal oscillation output circuit.

In developing a monolithic semiconductor
35 integrated circuit for television receivers, having a video intermediate-frequency amplifier, a video detector, and a synchronous separator formed in a single semiconductor chip, it has been found that the output response of a
40 synchronous separator circuit in a television receiver takes the form of sharp pulse-like waveforms, and has a large output voltage. Therefore, if a high-frequency amplifier circuit such as a video intermediate-frequency ampli-
45 fier and the synchronous separator circuit are constructed in the form of a single monolithic semiconductor integrated circuit, harmonic components of the synchronous pulse are fed back to the high-frequency amplifier circuit,
50 giving rise to the occurrence of oscillation and cross talk. To prevent such disadvantages, therefore, the high-frequency high-gain circuit and the synchronous separator circuit have to be constructed in the form of separate mono-
55 lithic semiconductor integrated circuits.

According to the present invention there is provided a monolithic semiconductor integrated circuit for television receivers including:

60 a high-frequency amplifier circuit for amplifying video intermediate-frequency signals, an input terminal of said high-frequency amplifier circuit being connected to a first externally located input terminal of said monolithic
65 semiconductor integrated circuit;

a video detector circuit which receives the output signals of said high-frequency amplifier circuit and produces composite video signals as detected outputs;

70 a synchronous separator circuit which receives the detected outputs of said video detector circuit and produces synchronous separation output signals to a first externally located output terminal of said monolithic
75 semiconductor integrated circuit; and

a first low-pass filter connected between said externally located output terminal and the output of said synchronous separator circuit, the time constant of said low-pass filter being
80 selected so that the resulting synchronous separation output signals have a pulse width approximately equal to the pulse width of horizontal synchronous pulses in said composite video signals and have reduced harmonic
85 components of said horizontal synchronous pulses.

Preferably, the high frequency amplifier circuit is a multistage amplifier circuit.

According to one embodiment of the present invention, the integrated circuit further includes a video amplifier circuit, the synchronous separator circuit receiving the detected
90 outputs of the video detector circuit via the video amplifier circuit.

95 In such an embodiment, the integrated circuit preferably further includes; an automatic gain control detector circuit which receives composite video signals from the video amplifier circuit, the gain of the high-frequency
100 amplifier circuit being controlled by an automatic gain control voltage produced by the automatic gain control detector circuit; and an automatic gain control amplifier circuit which receives the automatic gain control voltage
105 and produces a delay gain control voltage to a second externally located output terminal of the monolithic semiconductor integrated circuit.

The present invention will now be described
110 in greater detail, by way of example, with reference to the accompanying drawings, wherein:

Figure 1 is a circuit diagram of an embodiment of a synchronous separator circuit in a
115 monolithic semiconductor integrated circuit for television receivers according to the present invention;

Figure 2 is a block diagram of an embodiment of a signal processing circuit formed in
120 the monolithic semiconductor integrated circuit for television receivers according to the present invention;

Figure 3 is a cross-sectional view of a transistor and a capacitor in the synchronous
125 separator circuit in the monolithic semiconductor integrated circuit for television receivers according to the embodiment of the synchronous separator circuit shown in Fig. 1;

Figures 4(A) to 4(D) show signal waveforms
130 in circuit blocks of the signal processing circuit.

cuit shown in Fig. 2; and

Figure 5 shows an internal circuit and an external peripheral circuit of a signal processing circuit formed in the monolithic semiconductor circuit for television receivers according to the embodiment of the signal processing circuit shown in Fig. 2.

Referring first to Fig. 1, the synchronous separator circuit consists of a base-time-constant-type synchronous separator transistor circuit 1, an output gain enhancing circuit 2, a low-pass filter 3 and an emitter-follower output circuit Q_4 and R_6 .

According to this base-time-constant synchronous separator transistor circuit 1, a pnp transistor Q_1 operates as a synchronous separator transistor, a voltage divided by resistors R_2 and R_3 is used as a base biasing voltage, a composite video signal V_{in} is introduced through a series circuit consisting of a resistor R_1 and a capacitor C_1 , and a synchronous signal V_{sync} is obtained from the composite video signal produced at the collector electrode of the transistor Q_1 .

The transistor Q_1 is rendered conductive by the level V_p of a peak value of the synchronous signal in the composite video signal, whereby the capacitor C_1 is electrically charged. After the synchronous signal passed through, the electric charge stored in the capacitor C_1 is discharged through the resistors R_2 and R_3 . If the time constant for discharge is set to be greater than a horizontal period, the transistor Q_1 is rendered nonconductive for the period in which the video signal is being introduced. Therefore, the synchronous signal V_{sync} can be extracted from the collector electrode of the transistor Q_1 .

The output gain enhancing circuit 2 and the resistor R_6 form a collector load for the synchronous separator transistor Q_1 .

The output gain enhancing circuit consists of a transistor Q_2 connected in a diode configuration, a resistor R_4 connected to the emitter electrode of the transistor Q_2 , a transistor Q_3 the base electrode of which is connected to the base electrode of the transistor Q_2 and the collector electrode of which is connected to a power-supply terminal V_{cc} , and a resistor R_5 connected to the emitter electrode of the transistor Q_3 . The other ends of the resistors R_4 and R_5 are both connected to the resistor R_6 .

In the circuit 2, if the transistors Q_2 and Q_3 are of identical type emitter currents will flow in inverse proportion to the resistances of the emitter resistors R_4 and R_5 . For instance, if the ratio of the resistance R_4 to the resistance R_5 is set to be 4 to 1, the emitter current of the transistor Q_3 will be four times greater than the emitter current of the transistor Q_2 . The emitter current of the transistor Q_2 is determined by the collector current of the synchronizing separator transistor Q_1 . Hence, the sum of the currents in the two transistors Q_2

and Q_3 , which flows into the load resistor R_6 , is five times greater than the output current of the transistor Q_1 ; hence, the gain of the transistor Q_1 is substantially enhanced.

A resistor R_7 and a capacitor C_2 connected to the collector electrode of the transistor Q_1 constitute a low-pass filter 3 which removes harmonic components of the synchronous pulse obtained from the collector electrode of the transistor Q_1 . Particularly, when the synchronous separator circuit and the video intermediate-frequency amplifier circuit are to be constructed in the form of a single monolithic semiconductor integrated circuit, the time constant should be selected so that harmonic components close to the video intermediate-frequency signals, or harmonic components close to, for example, 58.75 MHz are removed.

An emitter-follower output circuit consists of a transistor Q_4 to which is fed the synchronous pulses via the low-pass filter 3, and an emitter resistor R_8 for the transistor Q_4 .

The synchronous pulses V_{sync} obtained through the emitter-follower output circuit describe an output waveform having a pulse width P_H , nearly equal to the pulse width P_H of the horizontal synchronizing signals without containing harmonic components as shown in the Figure.

Even when the synchronous separator circuit, consisting of transistors Q_1 to Q_4 , resistors R_1 to R_8 and capacitor C_2 , is formed in a monolithic semiconductor integrated circuit 13 containing video intermediate-frequency amplifier circuits 5 to 7 which are high-frequency high-gain circuits as shown in Fig. 2, synchronous pulses from which harmonic components have been removed are produced at a synchronous separator output terminal P_3 . Therefore, the quantity of high-frequency components fed back to the input terminal P_1 of the video intermediate-frequency amplifier circuit 5 can be greatly reduced despite the presence of capacitive coupling between terminals in the monolithic semiconductor integrated circuit. Consequently the problem such as oscillation does not occur.

A time-constant circuit 1' on the outer side of the integrated circuit is composed of voltage-dividing resistors R_2 and R_3 , a resistor R_1 , and a capacitor C_1 , which are connected in series.

Thus, as shown in Fig. 2, the monolithic semiconductor integrated circuit 13 for television sets incorporates a video intermediate-frequency amplifier circuit made up of a first video intermediate-frequency amplifier circuit 5, a second video intermediate-frequency circuit 6, a third video intermediate-frequency circuit 7, a video detector circuit 8 which receives the output of the video intermediate-frequency amplifier circuit, a video amplifier circuit 9 which receives the output of the video detector circuit 8, a noise canceller

circuit 10 which receives the output of the video amplifier circuit 9, an automatic gain control (hereinafter abbreviated to AGC) detector circuit 11 which receives the composite video signals via the noise canceller circuit 10, a synchronous separator circuit 4, and an AGC amplifier circuit 12 which receives the output of the AGC detector circuit 11.

An intermediate-frequency output of a tuner circuit (not shown) is applied to the input terminal P_1 of the first video intermediate-frequency amplifier circuit 5. The gain of each of the first, second and third video intermediate-frequency amplifier circuits 5, 6 and 7 are controlled by the output of the AGC detector circuit 11. The AGC amplifier circuit 12 compares an internal reference voltage with an output voltage from the AGC detector circuit 11, and gives a gain control signal to the tuner circuit via an externally located terminal P_2 .

The output of the synchronous separator circuit is obtained through the externally located terminal P_3 ; synchronous pulses (horizontal synchronous pulses) will also be sent to a horizontal automatic frequency control circuit (hereinafter abbreviated to AFC circuit), horizontal oscillation circuit through the externally located terminal P_3 .

An externally located terminal P_4 is to obtain composite video signals which are fed to the video amplifier circuit, and band pass amplifier circuit.

The circuit 1a having the same time constant as that determined by the resistors R_1 to R_3 and the capacitor C_1 shown in Fig. 1 is connected between the terminal P_4 and a terminal P_5 of the semiconductor integrated circuit 13. Therefore, a circuit similar to the circuit consisting of transistors Q_1 to Q_3 , resistors R_4 to R_8 , and capacitor C_2 of Fig. 1 incorporated in the semiconductor integrated circuit 13, produces synchronous separation signals to the terminal P_3 .

The horizontal synchronous pulses sent to the horizontal AFC circuit and to the horizontal oscillation circuit (not shown) can be obtained from the output terminal P_3 via a high-pass filter (differentiation circuit) 14 outside the integrated circuit 13. The vertical synchronous pulses sent to the vertical AFC circuit and to the vertical oscillation circuit (not shown), on the other hand, can be obtained from the output terminal P_3 via a low-pass filter (integrated circuit) 15 and a slicer circuit 16 outside the integrated circuit 13.

Figs. 4(A) to 4(D) show signal waveforms of circuit blocks shown in Fig. 2, in which the Fig. 4(A) shows signal waveforms (composite video signals) V_{in} obtained from the output terminal P_4 of the video amplifier circuit 9, Fig. 4(B) shows synchronous signals V_{out} obtained from the output terminal P_3 of the synchronous separator circuit 4, wherein the synchronous signals V_{out} include vertical syn-

chronous signals of a width of a period $P'v$, Fig. 4(C) shows output waveforms of the low-pass filter 15, and Fig. 4(D) shows a vertical synchronous pulse produced by the slicer circuit 16, wherein the vertical synchronous pulse has a pulse width of a period $P'v$ which is nearly equal to a period $P'v$ of the vertical synchronous signals.

The capacitor C_2 of the low-pass filter 3 shown in Fig. 1 may be connected between the base electrode of the transistor Q_4 of the emitter-follower output circuit and earth. With respect to the semiconductor integrated circuit, however, it is preferable to connect the capacitor C_2 between the base electrode of the transistor Q_4 and the power-supply terminal as shown in Fig. 1. In this case, the resistors R_7 , R_8 , capacitor C_2 and transistor Q_4 can be formed in the same semiconductor region, instead of being formed in semiconductor regions which are electrically isolated from each other. Therefore, areas of semiconductor regions for electrical isolation need not be provided.

Fig. 3 is a cross-sectional view of the transistor Q_4 and capacitor C_2 in the semiconductor integrated circuit. In Fig. 3, there is shown a p-type silicon substrate 20, an n⁺-type buried layer 21, an n-type epitaxial-growth layer 22 formed on the substrate 20, and a p⁺-type isolation region 23. A portion 22' in the n-type epitaxial-growth layer 22 is electrically isolated from other portions by means of the p-type silicon substrate 21 and the p⁺-type isolation region 23.

The capacitor C_2 consists of a pn-junction capacitance between the n-type layer 22' and a p-type region 25. The transistor Q_4 consists of the n-type layer 22' that serves as a collector, a p-type base region 26, and an n⁺-type emitter region 27.

On the surface of the n-type layer 22 a silicon oxide film 24 is formed. On the silicon oxide film leads 29, 30 and 31 are formed composed of an aluminium film.

The p-type region 25 is formed, for example, simultaneously with the base region 26 of the transistor Q_4 . Although not shown in Fig. 3, the resistors R_7 and R_8 are formed as p-type semiconductive resistance regions on the surface of the n-type layer 22' simultaneously with the base region 26.

As previously described, the television receiver circuits that are formed in two or three chips, can be formed in one chip according to the present invention. Therefore, the number of parts forming the television receiver circuits can be reduced, to decrease the manufacturing cost and to increase the reliability.

The present invention is not, of course, limited to the abovementioned embodiment. Any synchronous separator circuit may be formed in the single monolithic semiconductor integrated circuit together with the high-frequency high-gain circuit, provided the output

portion is equipped with a low-pass filter.

Also, the circuits other than the high-frequency high-gain circuits and synchronous separator circuits, may be combined in a variety of ways.

Fig. 5 shows an internal circuit of the signal processing circuit formed in a monolithic semiconductor integrated circuit according to the embodiment of the present invention shown in Fig. 2, and the associated external peripheral circuits. The circuit elements within a broken line IC are formed in a single silicon chip. On the other hand, the circuit elements outside the broken line IC are discrete elements located outside the semiconductor integrated circuit.

The video intermediate-frequency output signals of a tuner of a television receiver are fed to input terminals 1 and 16 of the integrated circuit via a band pass filter having predetermined band pass characteristics (for example, 54.25 to 60.25 MHz). The secondary terminals of a video intermediate-frequency transformer L_1 forming a portion of the band pass filter, are connected to the input terminals 1 and 16 via input coupling capacitors C_{10} and C_{11} .

The first video intermediate-frequency amplifier circuit 5' consists of transistors Q_{10} to Q_{14} , diodes D_1 and D_2 , and resistors R_{10} to R_{19} . The video intermediate-frequency signals applied to the input terminals 1 and 16 are then applied to the bases of a pair of differential transistors Q_{12} and Q_{13} via emitter-follower transistors Q_{10} and Q_{11} . The differential output signals of the first video intermediate-frequency amplifier circuit 5' are generated on the load resistors R_{18} and R_{19} , and are transmitted to the second video intermediate-frequency amplifier circuit 6'.

The AGC signals sent from the AGC detector circuit 11' to the terminal 6 are applied to a series circuit of resistor R_{30} and transistor Q_{29} . As the AGC signals increase, the current flowing into the series circuit is increased. The increase in current causes an increase in the collector current of a current source transistor Q_{14} in the first video intermediate-frequency amplifier circuit 5'. When the collector current increases above a predetermined value, the diodes D_1 and D_2 are rendered conductive. The dynamic resistances of the diodes D_1 and D_2 when the diodes D_1 and D_2 are rendered conductive is decreased with the increase in the collector current, whereby the voltage gain of the first video intermediate-frequency amplifier circuit 5' is increased. When the collector current is below the predetermined value, the diodes D_1 and D_2 are rendered non-conductive. In this case, the voltage gain is determined by the resistances R_{18} and R_{19} connected to the emitter electrodes of the pair of differential transistors Q_{12} and Q_{13} , whereby the voltage gain is decreased.

The second video intermediate-frequency

amplifier circuit 6' consists of transistors Q_{15} to Q_{19} , diodes D_3 and D_4 , and resistors R_{20} to R_{28} , and the third video intermediate-frequency amplifier circuit 7' consists of transistors Q_{20} to Q_{24} , diodes D_5 and D_6 , and resistors R_{27} to R_{33} . These circuits 6' and 7' operate in the same manner as the first video intermediate-frequency amplifier circuit 5' previously described. Therefore, their operation is not described in detail.

The differential output signals of the third video intermediate-frequency amplifier circuit 7' are transmitted to the video detector circuit 8' via emitter-follower transistors Q_{25} and Q_{26} .

A power-supply terminal 12 receives a power-supply voltage V_{CC} which is divided by the resistors R_{36} and R_{37} . The thus divided voltage is supplied as an operation voltage to the first, second and third intermediate-frequency amplifier circuits 5', 6' and 7' via emitter-follower transistors Q_{27} and Q_{28} connected in Darlington configuration.

The video detector circuit 8' consists of transistors Q_{31} and Q_{31} to Q_{41} , diodes D_7 and D_8 , resistors R_{38} to R_{45} , and a resonance circuit (formed by L_2 , C_{12} and R_{46}) which is connected between terminals 8 and 9 of the integrated circuit and which is tuned to 58.75 MHz. The detector circuit of this type is called synchronous low-level detector, and has been disclosed in the IEEE TRANSACTIONS ON BROADCAST AND TELEVISION RECEIVERS, Vol. BTR-15, No. 2, pp. 159-166, published in July, 1969.

The video detected outputs obtained on the resistors R_{44} and R_{45} are transmitted to the first video amplifier circuit 9'a. The first video amplifier circuit 9'a consists of transistors Q_{42} to Q_{51} , and resistors R_{46} to R_{51} , and produces an output signal on the collector electrode of the transistor Q_{44} . The output signal is transmitted to the second video amplifier circuit 9'b which consists of transistors Q_{52} to Q_{58} , and diodes D_9 and D_{10} , and which produces a composite video signal V_{in} (as shown in the Fig. 4(A) at the terminal 11).

A first biasing circuit 17' consisting of transistors Q_{59} to Q_{61} , diodes D_{11} , D_{12} and D_{13} , a zener diode ZD_1 , and resistors R_{62} to R_{64} , a second biasing circuit 18' consisting of transistors Q_{62} and Q_{63} , and resistors R_{65} to R_{69} , and a third biasing circuit 19' consisting of transistors Q_{64} to Q_{68} , and resistors R_{60} to R_{63} , respectively supply biasing voltages to various circuits in the integrated circuit.

The composite video signal V_{in} transmitted to the terminal 11 is fed to a synchronous separator input terminal 14. A circuit network consisting of a diode D_{14} , resistors R_{71} to R_{73} , R_{64} , and capacitors C_{11} , C_{13} and C_{14} is connected between the terminals 11 and 14. The diode D_{14} in the circuit network reduces negative pulse-like noises contained in the composite video signals V_{in} .

Thus, the composite video signals V_{in} are

applied to the base of the transistor Q_1 in the synchronous separator circuit 1' via a series circuit consisting of the resistor R_1 and the capacitor C_1 . The operation of the output gain enhancing circuit 2' and the operation of the low-pass filter are the same as those of Fig. 1, and are not described further. The capacitor C_2 and the output transistor Q_4 of the low-pass filter 3' have been formed in the monolithic integrated circuit as shown in Fig. 3.

Thus, the synchronous separator output signals V_{sync} having a pulse width P'_H approximately equal to the pulse width P_H of the horizontal synchronous signals in the composite video signals V_{in} are produced from a synchronous separator output terminal 13. The time constant of the low-pass filter 3' has been set to such a value that the abovementioned pulse width P'_H is obtained and harmonic components are removed from the horizontal synchronous pulse signals. Hence, since it is possible to greatly reduce the quantity of harmonic components fed back from the synchronous separator output terminal 13 to the input terminals 1 and 16 of the first video intermediate-frequency amplifier circuit 5', unstable factors such as oscillation and cross talk can be removed.

The noise canceller circuit 10' consists of transistors Q_{67} to Q_{75} , zener diode ZD_2 , resistors R_{65} to R_{71} and R_{73} , and capacitors C_{16} to C_{18} .

The AGC detector circuit 12' consists of transistors Q_{76} to Q_{86} , diode D_{15} , resistors R_{74} to R_{82} , and capacitor C_{19} .

The composite video signals obtained from the collector electrode of the transistor Q_{54} of the second video amplifier circuit 9b are fed to the base electrode of the transistor Q_{76} of an AGC detector circuit 11' via resistors R_{65} and R_{66} and base-emitter junction of the transistor Q_{67} in the noise canceller circuit 10'.

The composite video signals are amplified by the pair of differential transistors Q_{76} and Q_{77} and the common emitter transistor Q_{79} of the AGC detector circuit 11', and are fed to the base electrode of the transistor Q_{80} . The transistor Q_{80} , resistors R_{76} and R_{80} , and capacitor C_{19} work as an emitter-follower-type detector for detecting peak values of horizontal synchronous pulse signals in the composite video signals. Therefore, the terminal 5 of the integrated circuit is maintained at a voltage approximately equal to the peak value of the horizontal synchronous pulse signals. The voltage is amplified by a pair of differential transistors Q_{81} and Q_{82} of the AGC detector circuit 11', and is fed as an AGC voltage to the terminal 6 via current-mirror transistors Q_{84} and Q_{85} .

When the AGC voltage fed from the AGC detector circuit 11' to the terminal 6 is applied to a series circuit consisting of resistor R_{30} and transistor Q_{29} , the voltage gain of each of the first, second and third video

intermediate-frequency amplifier circuits 5', 6' and 7' are controlled, as previously described.

The composite video signals obtained from the collector electrode of the transistor Q_{54} in the second video amplifier circuit 9'b, on the other hand, are supplied to the base of the transistor Q_{73} via the resistors R_{65} and R_{66} and base-emitter junction of the transistor Q_{67} in the noise canceller circuit 10'. Therefore, the voltage of the capacitor C_{18} (voltage of terminal 10) to which is connected the emitter electrode of the transistor Q_{73} via resistor R_{69} is maintained at an average value of the composite video signals. The average voltage is applied to the base electrode of the transistor Q_{69} via the base-emitter junction of the transistor Q_{74} and the resistor R_{70} .

The composite video signals obtained from the emitter electrode of the transistor Q_{55} of the second video amplifier circuit 9'b are applied to the base electrode of the transistor Q_{68} of the noise canceller circuit 10' via the resistor R_{68} . Therefore, when the composite video signals contain negative-going noise pulses smaller than the average voltage applied to the base of the transistor Q_{69} , the transistor Q_{68} is turned "off" and the transistor Q_{69} is turned "on" during the period of the noise pulses. Consequently, a heavy current flows into the current-mirror transistors Q_{71} and Q_{72} , causing the transistor Q_{67} to be turned "on". When the transistor Q_{67} is rendered conductive, the transistor Q_{76} in the AGC detector circuit 11' is rendered conductive, and the transistors Q_{77} , Q_{79} and Q_{80} are rendered nonconductive.

Therefore, during the period of the negative-going pulses, the voltage maintained at the terminal 5 is not affected by the noise pulses. Consequently, the AGC voltage obtained from the terminal 6 is not affected by the noise pulses.

The AGC voltage of the terminal 6 is sent to an AGC amplifier circuit 12' via an RF delay-adjust circuit consisting of resistors R_{83} and R_{84} , and capacitors C_{20} and C_{21} , and the terminal 4. The AGC amplifier circuit 12' consists of transistors Q_{87} to Q_{97} , diodes D_{16} to D_{19} , zener diode ZD_3 , and resistors R_{85} to R_{90} , and produces, through the terminal 3, a delayed AGC signal for controlling the voltage gain of the radio-frequency amplifier circuit in the tuner (not shown).

When the AGC voltage at the terminal 6 is high, the transistors Q_{87} and Q_{88} of the AGC amplifier circuit 12' are rendered conductive, and the transistors Q_{89} to Q_{92} non-conductive. Hence, the delayed AGC voltage at the terminal 3 is determined by a relatively small voltage from the transistor Q_{93} .

When the AGC voltage at the terminal 7 is lowered, the conductivities of the transistors Q_{87} and Q_{88} are decreased, and the conductivities of the transistors Q_{89} to Q_{92} are increased, whereby the delay AGC voltage at

the terminal 3 is increased.

However, the rise of the delayed AGC voltage is limited by the breakdown voltage of the zener diode ZD_3 and by the forward voltage of the diode D_{18} .

CLAIMS

1. A monolithic semiconductor integrated circuit for television receivers including:
 - 10 a high-frequency amplifier circuit for amplifying video intermediate-frequency signals, an input terminal of said high-frequency amplifier circuit being connected to a first externally located input terminal of said monolithic
 - 15 semiconductor integrated circuit;
 - a video detector circuit which receives the output signals of said high-frequency amplifier circuit and produces composite video signals as detected outputs;
 - 20 a synchronous separator circuit which receives the detected outputs of said video detector circuit and produces synchronous separation output signals to a first externally located output terminal of said monolithic
 - 25 semiconductor integrated circuit; and
 - a first low-pass filter connected between said externally located output terminal and the output of said synchronous separator circuit, the time constant of said low-pass filter being
 - 30 selected so that the resulting synchronous separation output signals have a pulse width approximately equal to the pulse width of horizontal synchronous pulses in said composite video signals and have reduced harmonic
 - 35 components of said horizontal synchronous pulses.
 2. A monolithic semiconductor integrated circuit for television receivers according to claim 1, wherein said high-frequency amplifier
 - 40 circuit is a multistage amplifier circuit.
 3. A monolithic semiconductor integrated circuit for television receivers according to claim 1 or claim 2, further including a video
 - 45 amplifier circuit, said synchronous separator circuit receiving the detected output of said video detector circuit via said video amplifier circuit.
 4. A monolithic semiconductor integrated circuit for television receivers according to
 - 50 claim 3, further including:
 - an automatic gain control detector circuit which receives composite video signals from said video amplifier circuit the gain of said high-frequency amplifier circuit being controlled by an automatic gain control voltage
 - 55 produced by said automatic gain control detector circuit; and
 - an automatic gain control amplifier circuit which receives said automatic gain control
 - 60 voltage and produces a delay gain control voltage to a second externally located output terminal of said monolithic semiconductor integrated circuit.
 5. A monolithic semiconductor integrated
 - 65 circuit for television receivers according to

claim 4, further including a noise canceller circuit which is connected between said video amplifier circuit and said automatic gain control detector circuit.

- 70 6. A monolithic semiconductor integrated circuit for television receivers according to claim 5, further including an emitter-follower output circuit which is connected between said first low-pass filter and said first externally located output terminal.
- 75 7. A television receiver having a monolithic semiconductor integrated circuit according to any one of claims 1 to 5, including:
 - a first high-pass filter which is connected to
 - 80 said first externally located output terminal of said monolithic semiconductor integrated circuit to obtain horizontal synchronous signals; and
 - a second low-pass filter and a slicer circuit
 - 85 which are connected to said first externally located output terminal to obtain vertical synchronous signals.
8. A monolithic semiconductor integrated circuit for television receivers substantially as
- 90 herein described with reference to Figs. 1, 2 or 5 of the accompanying drawings.

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the terminal 3 is increased.

However, the rise of the delayed AGC voltage is limited by the breakdown voltage of the zener diode ZD₃ and by the forward voltage of the diode D₁₈.

CLAIMS

1. A monolithic semiconductor integrated circuit for television receivers including:
 - 10 a high-frequency amplifier circuit for amplifying video intermediate-frequency signals, an input terminal of said high-frequency amplifier circuit being connected to a first externally located input terminal of said monolithic semiconductor integrated circuit;
 - 15 a video detector circuit which receives the output signals of said high-frequency amplifier circuit and produces composite video signals as detected outputs;
 - 20 a synchronous separator circuit which receives the detected outputs of said video detector circuit and produces synchronous separation output signals to a first externally located output terminal of said monolithic semiconductor integrated circuit; and
 - 25 a first low-pass filter connected between said externally located output terminal and the output of said synchronous separator circuit, the time constant of said low-pass filter being selected so that the resulting synchronous separation output signals have a pulse width approximately equal to the pulse width of horizontal synchronous pulses in said composite video signals and have reduced harmonic components of said horizontal synchronous pulses.
2. A monolithic semiconductor integrated circuit for television receivers according to claim 1, wherein said high-frequency amplifier circuit is a multistage amplifier circuit.
3. A monolithic semiconductor integrated circuit for television receivers according to claim 1 or claim 2, further including a video amplifier circuit, said synchronous separator circuit receiving the detected output of said video detector circuit via said video amplifier circuit.
4. A monolithic semiconductor integrated circuit for television receivers according to claim 3, further including:
 - an automatic gain control detector circuit which receives composite video signals from said video amplifier circuit the gain of said high-frequency amplifier circuit being controlled by an automatic gain control voltage produced by said automatic gain control detector circuit; and
 - an automatic gain control amplifier circuit which receives said automatic gain control voltage and produces a delay gain control voltage to a second externally located output terminal of said monolithic semiconductor integrated circuit.
5. A monolithic semiconductor integrated circuit for television receivers according to

claim 4, further including a noise canceller circuit which is connected between said video amplifier circuit and said automatic gain control detector circuit.

6. A monolithic semiconductor integrated circuit for television receivers according to claim 5, further including an emitter-follower output circuit which is connected between said first low-pass filter and said first externally located output terminal.
7. A television receiver having a monolithic semiconductor integrated circuit according to any one of claims 1 to 5, including:
 - a first high-pass filter which is connected to said first externally located output terminal of said monolithic semiconductor integrated circuit to obtain horizontal synchronous signals; and
 - a second low-pass filter and a slicer circuit which are connected to said first externally located output terminal to obtain vertical synchronous signals.
8. A monolithic semiconductor integrated circuit for television receivers substantially as herein described with reference to Figs. 1, 2 or 5 of the accompanying drawings.

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