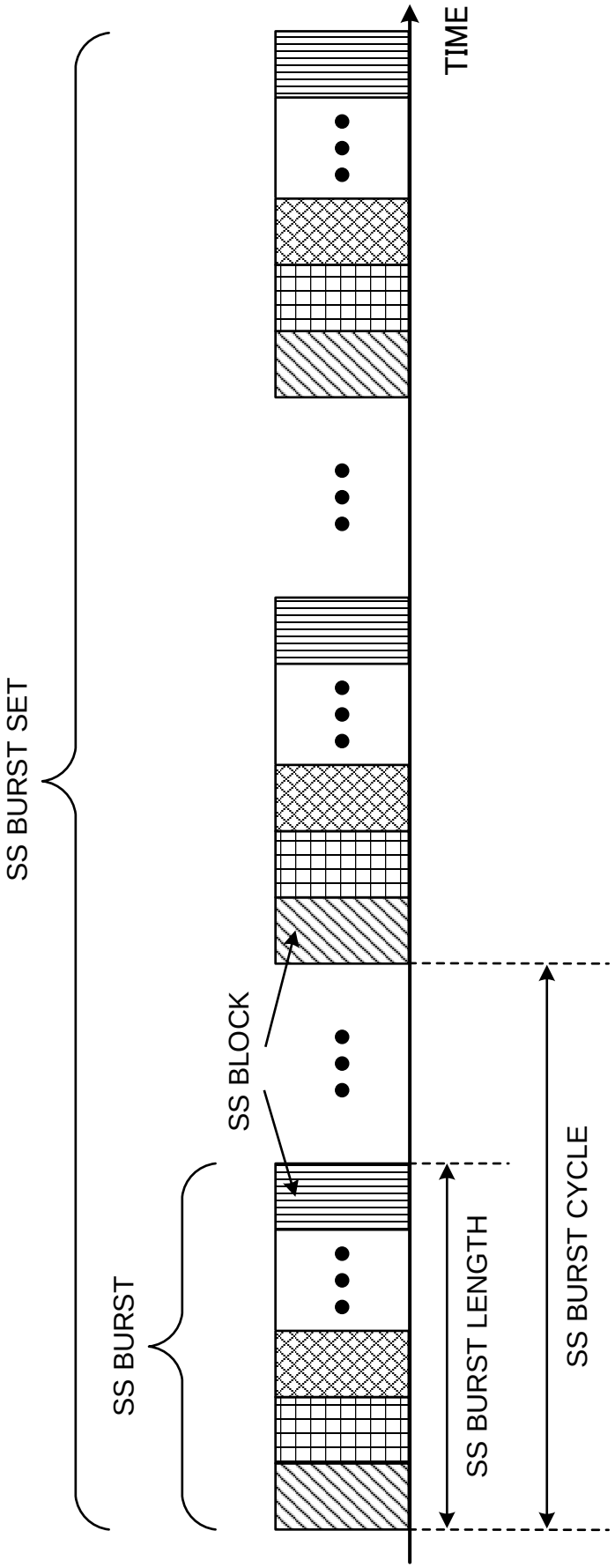

TIME
SS BURST SET
SS BLOCK
SS BURST
SS BURST LENGTH
SS BURST CYCLE

FIG. 1

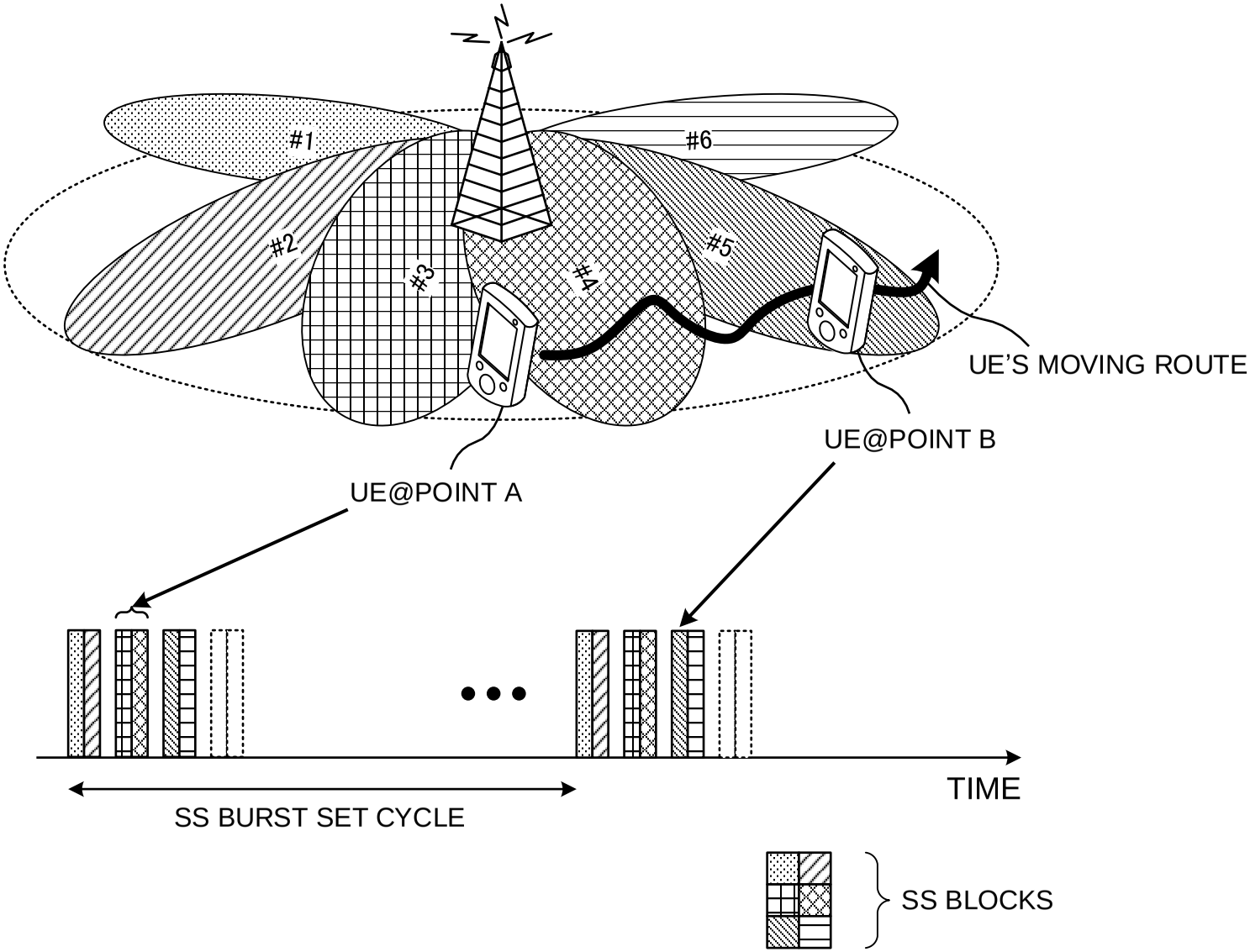

#1
#2
#3
#4
#5
#6
UE'S MOVING ROUTE
UE@POINT B
UE@POINT A
TIME
SS BURST SET CYCLE
SS BLOCKS

FIG. 2

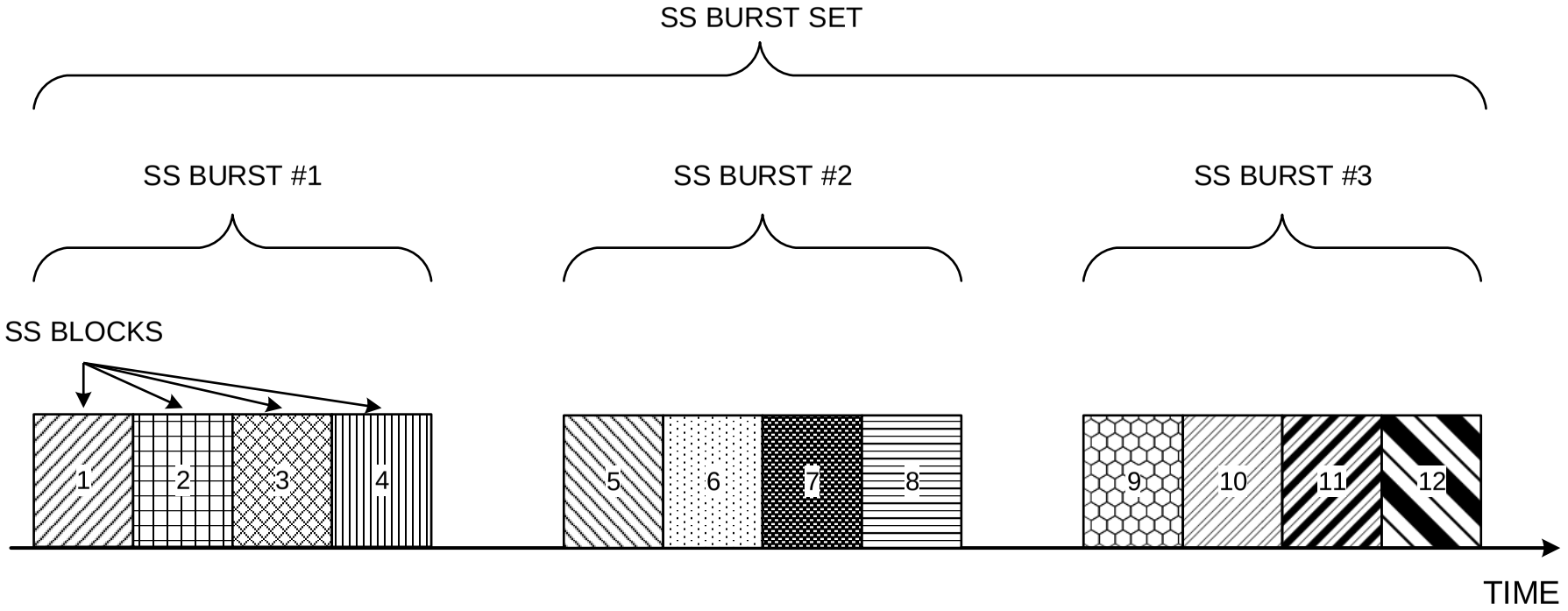

SS BURST SET
SS BURST #1
SS BURST #2
SS BURST #3
SS BLOCKS
1
2
3
4
5
6
7
8
9
10
11
12
TIME

FIG. 3

FIG. 4A

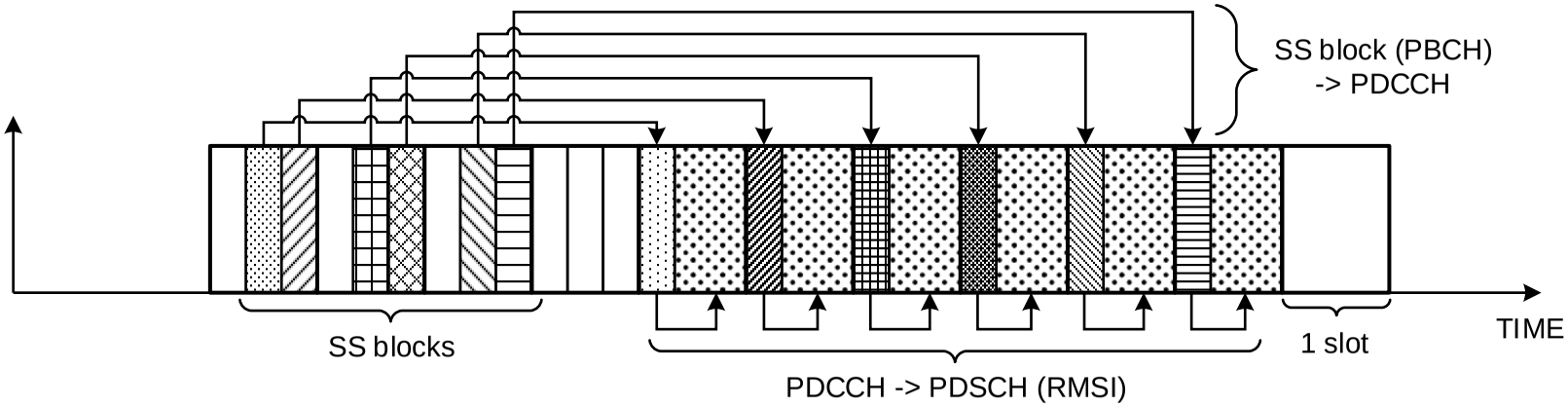


FIG. 4B

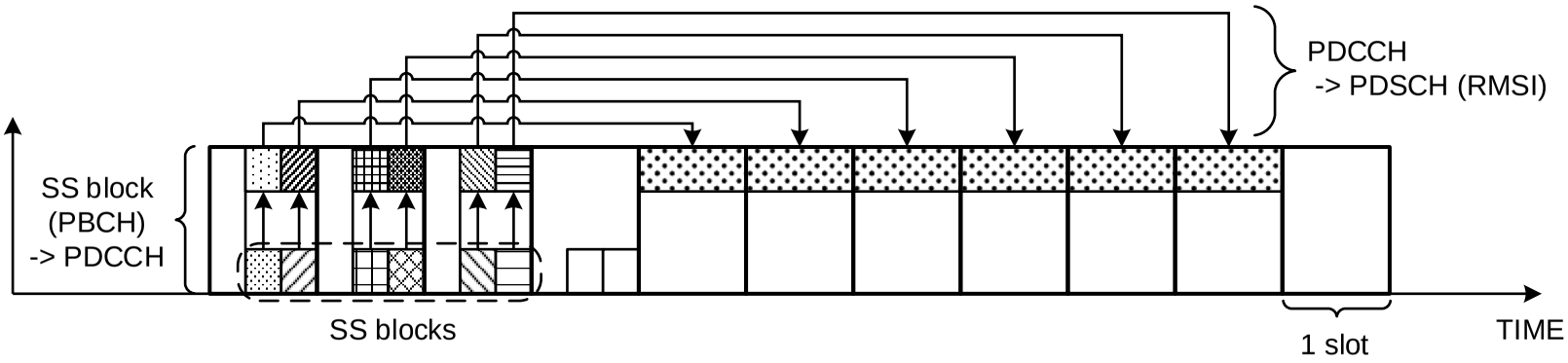


FIG. 4C

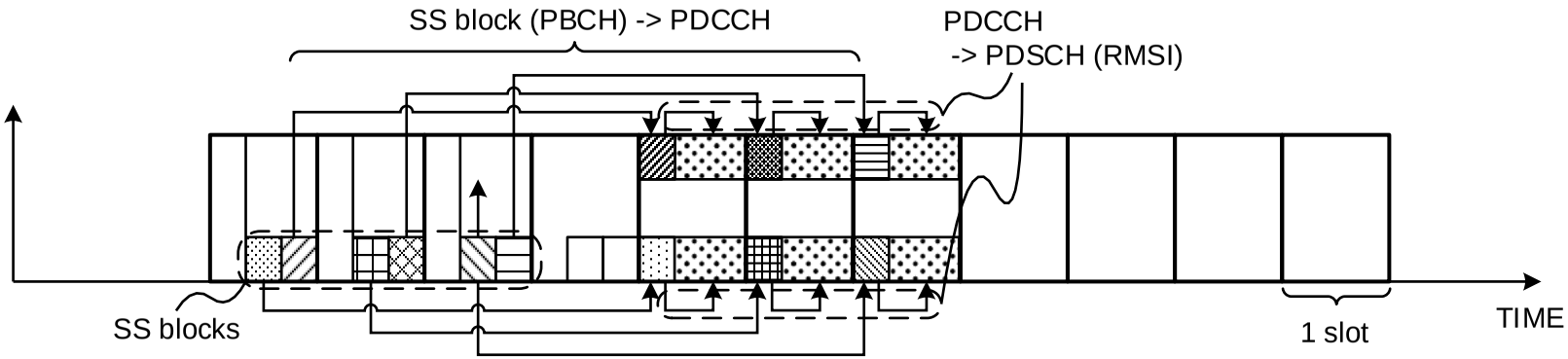


FIG. 5A

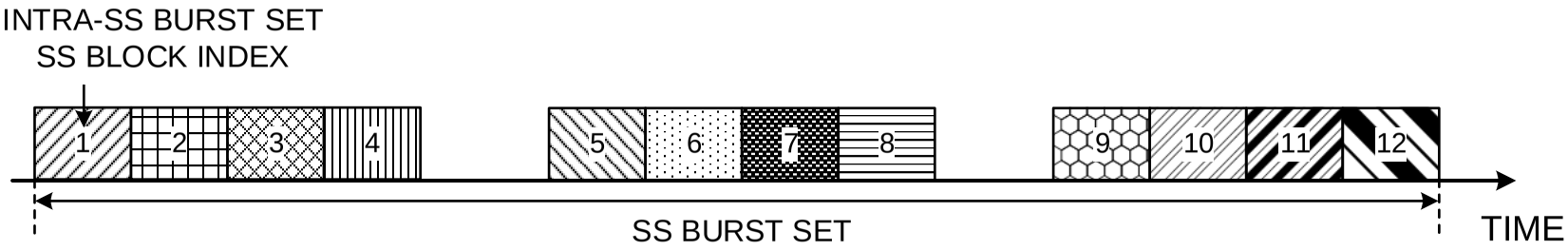


FIG. 5B

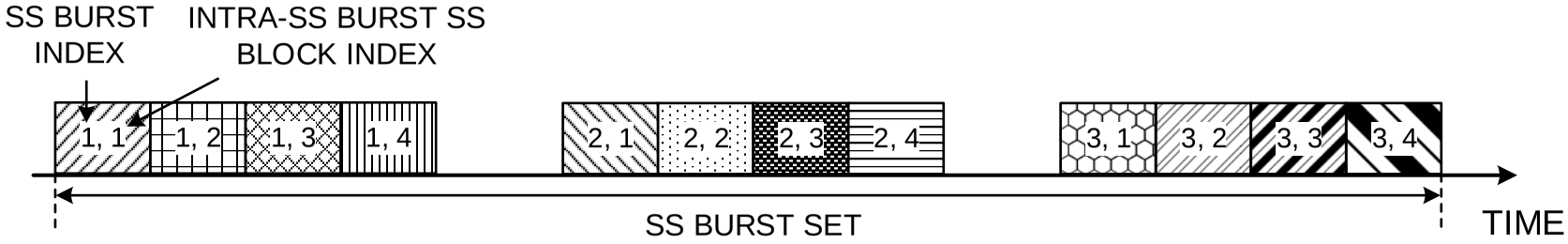


FIG. 5C

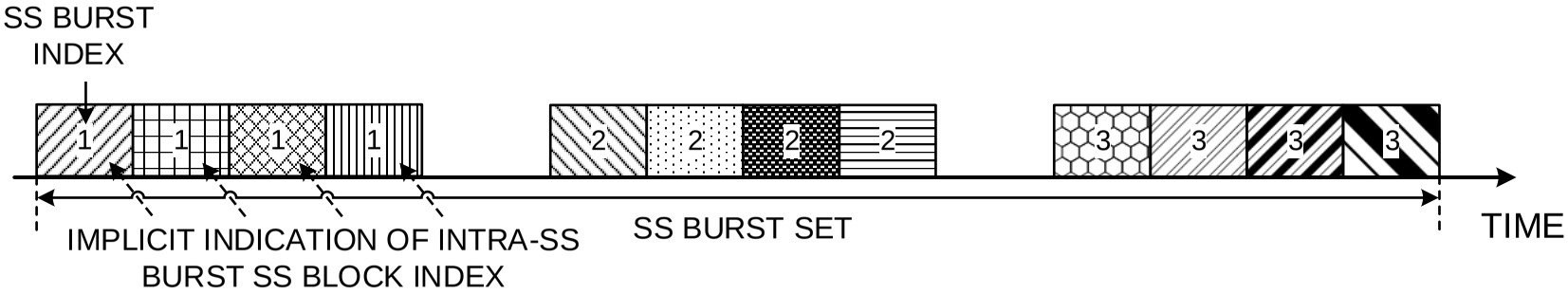
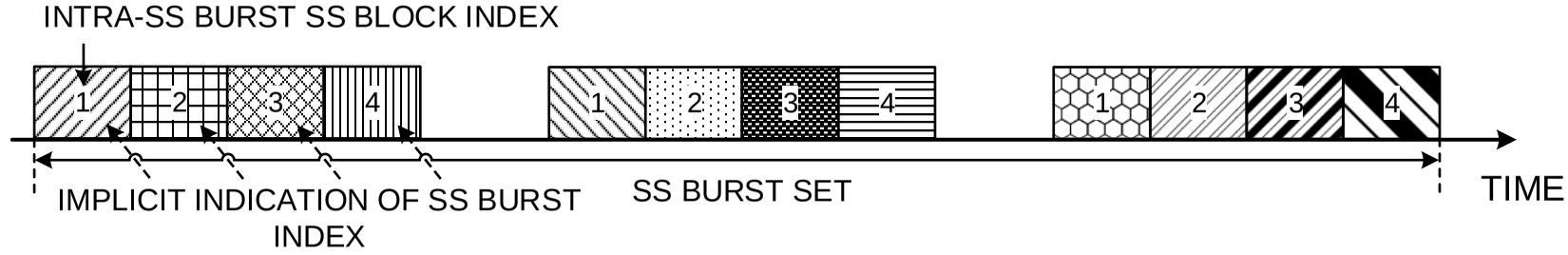


FIG. 5D



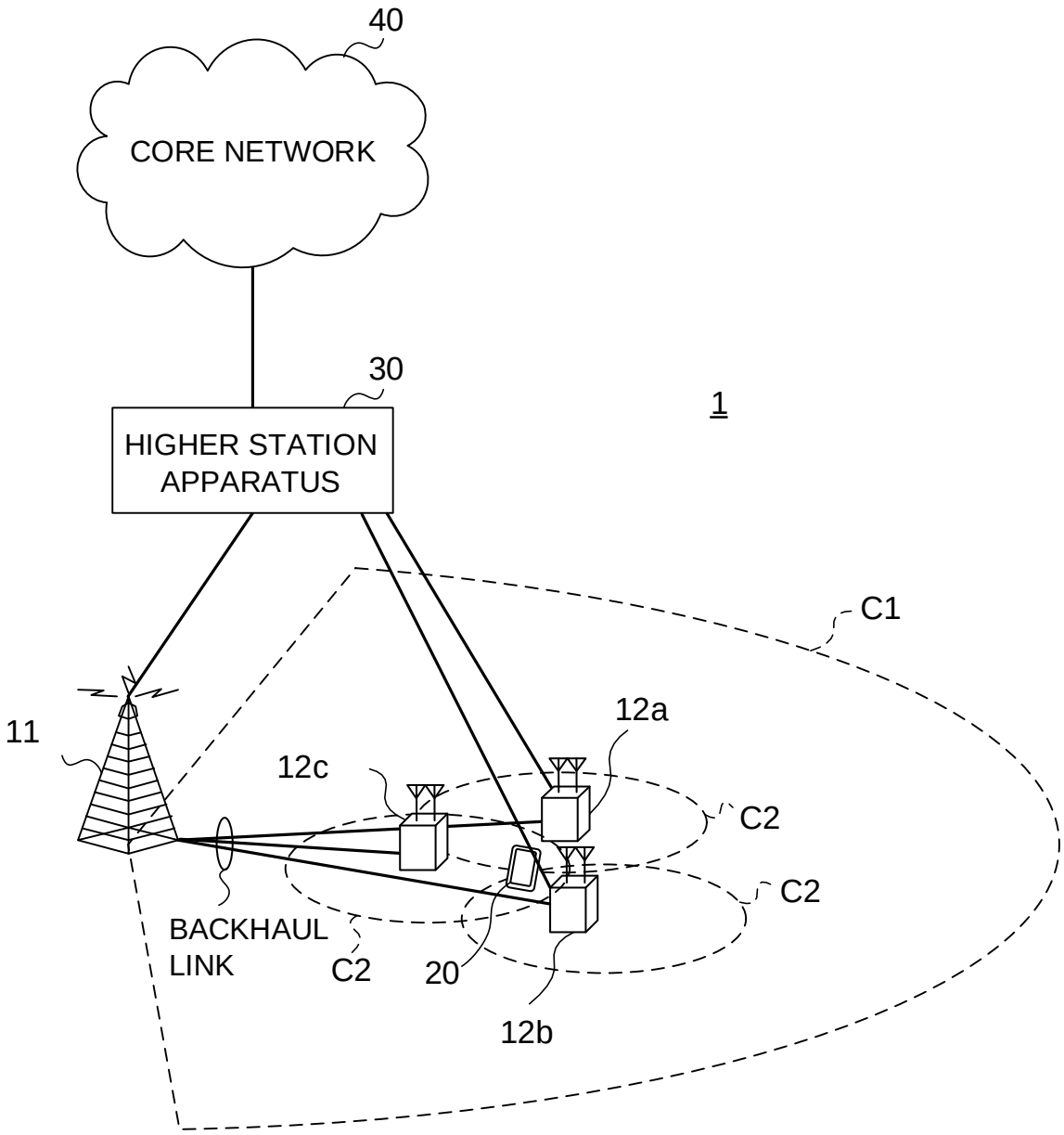

40
CORE NETWORK
30
HIGHER STATION APPARATUS
1
C1
11
12a
12c
C2
C2
BACKHAUL LINK
C2
20
12b

FIG. 6

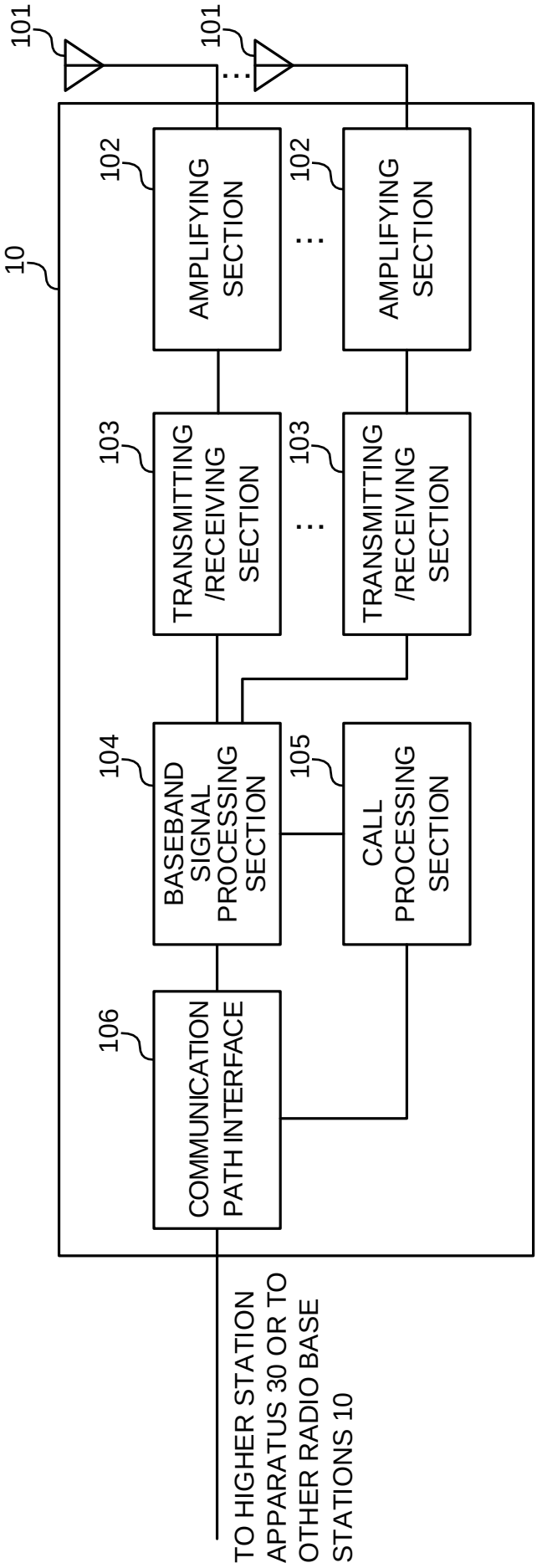

101
101
10
102
AMPLIFYING SECTION
102
AMPLIFYING SECTION
103
TRANSMITTING /RECEIVING SECTION
103
TRANSMITTING /RECEIVING SECTION
104
BASEBAND SIGNAL PROCESSING SECTION
105
CALL PROCESSING SECTION
106
COMMUNICATION PATH INTERFACE
TO HIGHER STATION APPARATUS 30 OR TO OTHER RADIO BASE STATIONS 10

FIG. 7

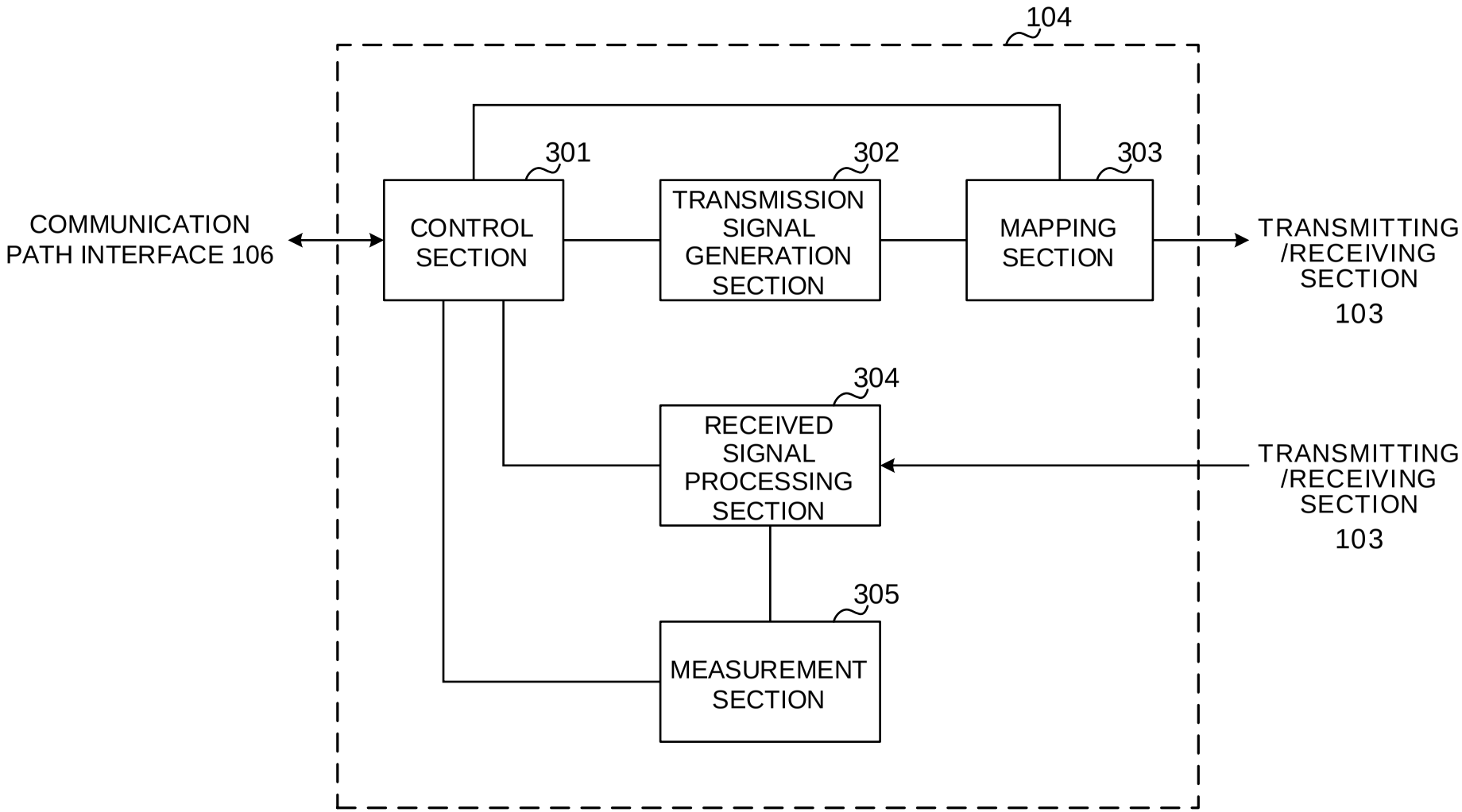

104
301
302
303
COMMUNICATION PATH INTERFACE 106
CONTROL SECTION
TRANSMISSION SIGNAL GENERATION SECTION
MAPPING SECTION
TRANSMITTING /RECEIVING SECTION
103
304
RECEIVED SIGNAL PROCESSING SECTION
TRANSMITTING /RECEIVING SECTION
103
305
MEASUREMENT SECTION

FIG. 8

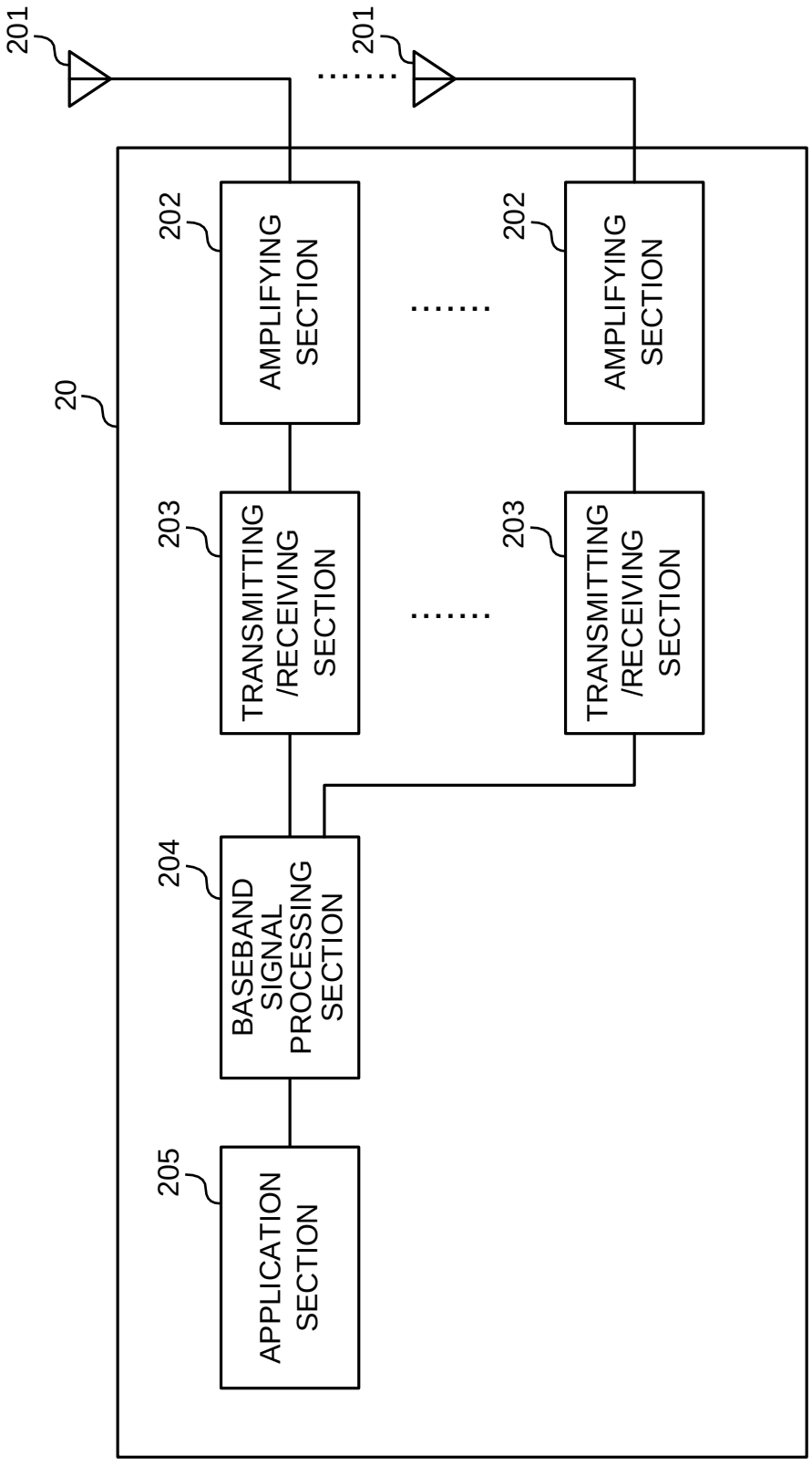

201
201
20
202
AMPLIFYING SECTION
202
AMPLIFYING SECTION
203
TRANSMITTING /RECEIVING SECTION
203
TRANSMITTING /RECEIVING SECTION
204
BASEBAND SIGNAL PROCESSING SECTION
205
APPLICATION SECTION

FIG. 9

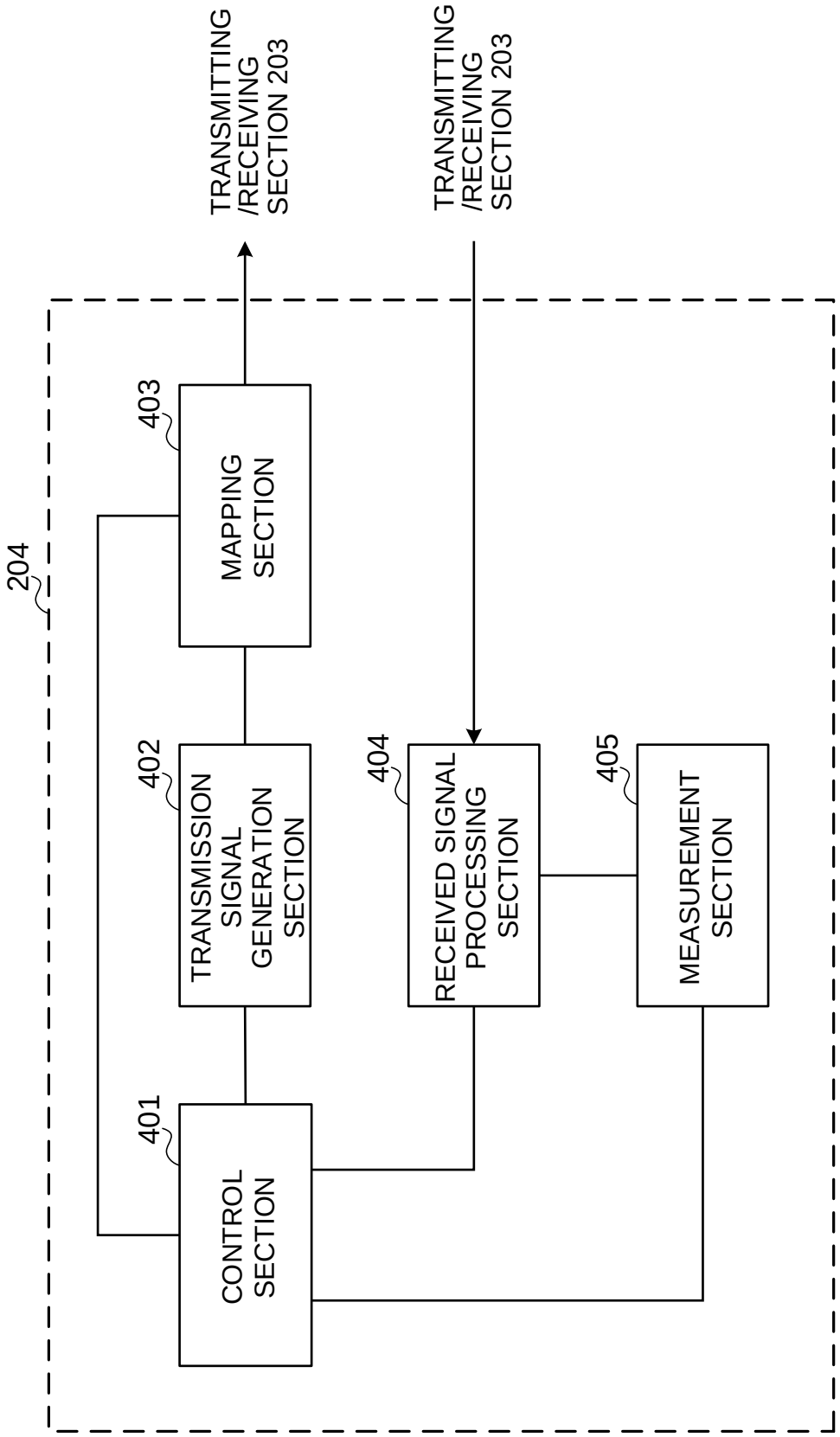

TRANSMITTING /RECEIVING SECTION 203
TRANSMITTING /RECEIVING SECTION 203
204
403
MAPPING SECTION
402
TRANSMISSION SIGNAL GENERATION SECTION
404
RECEIVED SIGNAL PROCESSING SECTION
405
MEASUREMENT SECTION
401
CONTROL SECTION

FIG. 10

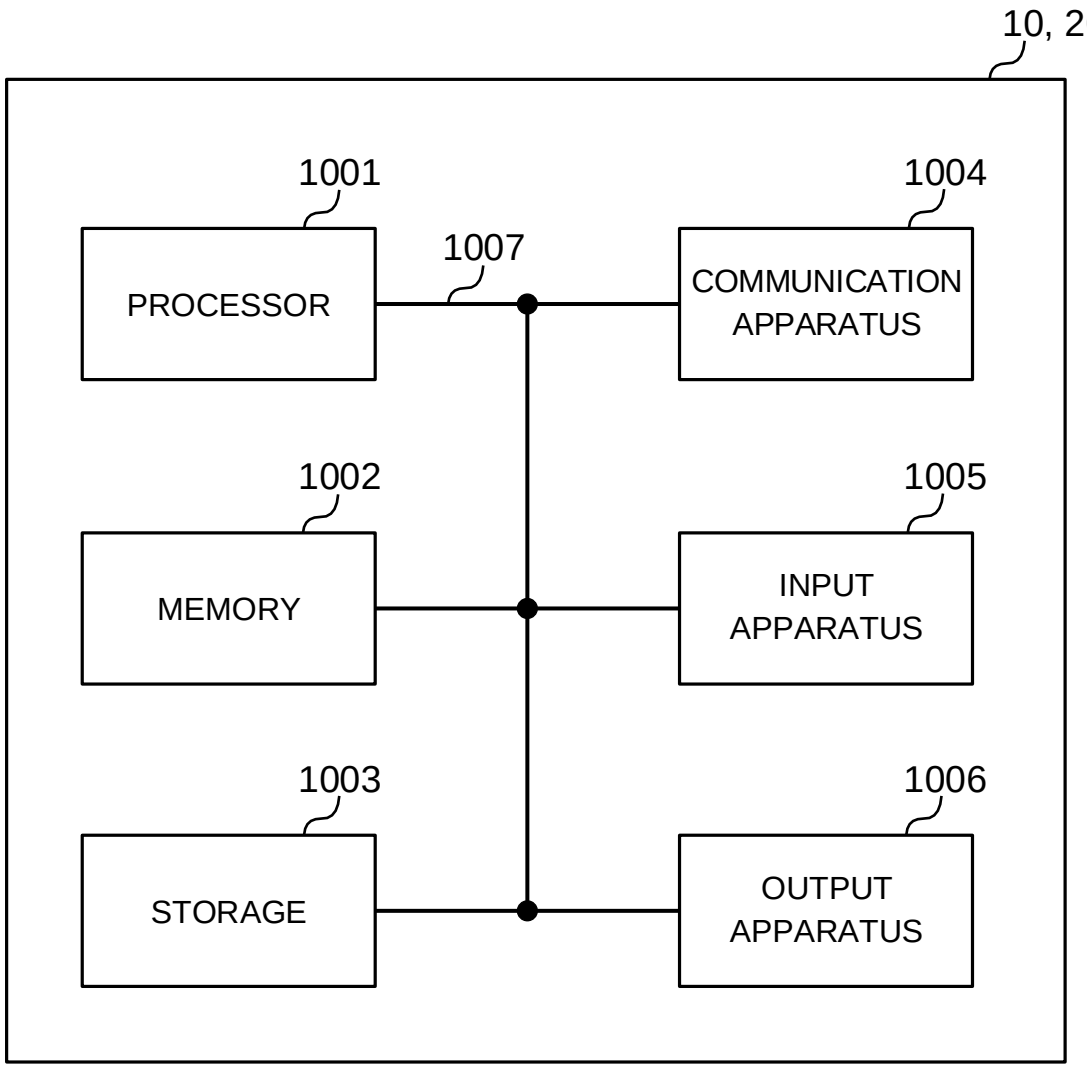

10, 20
1001
PROCESSOR
1007
1004
COMMUNICATION APPARATUS
1002
MEMORY
1005
INPUT APPARATUS
1003
STORAGE
1006
OUTPUT APPARATUS

FIG. 11