

SEMICONDUCTOR DEVICE HAVING AN EMBEDDED CONDUCTIVE LAYER FOR POWER/GROUND PLANES IN FO-EWLB

Field of the Invention

[0001] The present invention relates in general to semiconductor devices and, more particularly, to a semiconductor device and method of forming an embedded conductive layer to provide power/ground planes in a fan-out embedded wafer-level ball grid array (Fo-eWLB).

Background of the Invention

[0002] Semiconductor devices are commonly found in modern electronic products. Semiconductor devices vary in the number and density of electrical components. Discrete semiconductor devices generally contain one type of electrical component, e.g., light emitting diode (LED), small signal transistor, resistor, capacitor, inductor, and power metal oxide semiconductor field effect transistor (MOSFET). Integrated semiconductor devices typically contain hundreds to millions of electrical components. Examples of integrated semiconductor devices include microcontrollers, microprocessors, charged-coupled devices (CCDs), solar cells, and digital micro-mirror devices (DMDs).

[0003] Semiconductor devices perform a wide range of functions such as signal processing, high-speed calculations, transmitting and receiving electromagnetic signals, controlling electronic devices, transforming sunlight to electricity, and

Claims

What is claimed:

1. A semiconductor device, comprising:

a semiconductor die;

a ground plane disposed outside a footprint of the semiconductor die, wherein the semiconductor die includes a first side oriented toward the ground plane and a second side opposite the first side oriented away from the ground plane, and wherein the ground plane includes a thickness between a first surface and a second surface of the ground plane that is less than a width of the ground plane in a direction perpendicular to the thickness;

an encapsulant deposited over the semiconductor die and the ground plane, wherein a surface of the encapsulant is coplanar to the first surface of the ground plane and a first surface of the semiconductor die, and wherein the encapsulant completely covers the second surface of the ground plane and a second surface of the semiconductor die opposite the first surface of the semiconductor die;

an insulating layer formed directly on the surface of the encapsulant, the first surface of the semiconductor die, and the first surface of the ground plane;

a conductive layer formed directly on a surface of the insulating layer, wherein the conductive layer includes,

a first conductive trace electrically coupling the semiconductor die to the ground plane, and

a second conductive trace extending from the semiconductor die and over the ground plane without physically contacting the ground plane; and

a solder bump disposed directly on the conductive layer.

2. The semiconductor device of claim 1, further including an interconnect structure embedded within the encapsulant with the ground plane formed over a surface of the interconnect structure.

3. The semiconductor device of claim 2, wherein the interconnect structure includes a plurality of conductive vias.

4. The semiconductor device of claim 1, wherein the ground plane is disposed on a dummy die outside the footprint of the semiconductor die.

5. The semiconductor device of claim 1, further including a power plane formed as part of the conductive layer, wherein the ground plane and power plane form a decoupling capacitor.

6. The semiconductor device of claim 1, further including an interconnect structure formed over the conductive layer, wherein the second conductive trace extends to the interconnect structure and the interconnect structure is disposed over the ground plane.

7. The semiconductor device of claim 1, wherein the first conductive trace extends completely from the semiconductor die to the ground plane.

8. A semiconductor device, comprising:

a semiconductor die comprising an active surface and a back surface opposite the active surface;

a conductive plane disposed outside a footprint of the semiconductor die, wherein the semiconductor die includes a first side surface oriented toward the conductive plane and a second side surface oriented away from the conductive plane, and wherein the first side surface and second side surface are perpendicular to the active surface of the semiconductor die;

an encapsulant deposited over the semiconductor die and the conductive plane, wherein a surface of the encapsulant is coplanar to the active surface of the semiconductor die and a front surface of the conductive plane, and wherein the encapsulant completely covers the back surface of the semiconductor die and a back surface of the conductive plane opposite the front surface of the conductive plane;

a first conductive trace formed over the semiconductor die and the conductive plane, wherein the first conductive trace is electrically isolated from the conductive plane; and

a second conductive trace electrically extending from the front surface of the conductive plane to a ground terminal or a voltage terminal.

9. The semiconductor device of claim 8, further including a power plane disposed outside a footprint of the semiconductor die, wherein the conductive plane includes a ground plane, and wherein a surface of the power plane is coplanar with a surface of the conductive plane and the active surface of the semiconductor die.

10. The semiconductor device of claim 8, wherein the conductive plane is disposed on an interconnect structure.

11. The semiconductor device of claim 10, wherein the interconnect structure includes a substrate and a plurality of conductive vias formed through the substrate.

12. The semiconductor device of claim 8, wherein the conductive plane is disposed on a dummy die within a height of the semiconductor die.

13. The semiconductor device of claim 8, further including a conductive bump formed directly on a surface of the conductive plane, wherein the surface of the conductive plane is coplanar with the active surface of the semiconductor die.

14. A semiconductor device, comprising:

- a semiconductor die;

- a flat conductive plane disposed adjacent to the semiconductor die, wherein the semiconductor die includes a first side oriented toward the flat conductive plane and a second side oriented away from the flat conductive plane;

- an encapsulant deposited over the semiconductor die and the flat conductive plane, wherein a surface of the encapsulant is coplanar to a surface of the semiconductor die and a surface of the flat conductive plane;

- a first conductive trace formed over the surface of the encapsulant, the surface of the semiconductor die, and the surface of the flat conductive plane and electrically coupling the flat conductive plane to the semiconductor die; and

a second conductive trace extending over the flat conductive plane without physically contacting the flat conductive plane.

15. The semiconductor device of claim 14, wherein the flat conductive plane is disposed on an interconnect structure and the encapsulant is deposited over the flat conductive plane and interconnect structure.

16. The semiconductor device of claim 15, wherein the interconnect structure includes a substrate and a plurality of conductive vias formed through the substrate.

17. The semiconductor device of claim 14, wherein the flat conductive plane is disposed on a dummy die and the encapsulant is deposited over the flat conductive plane and the dummy die.

18. The semiconductor device of claim 14, further including an interconnect structure formed over the first conductive trace opposite the flat conductive plane.

19. The semiconductor device of claim 14, wherein the second conductive trace forms a microstrip line.

20. A semiconductor device, comprising:
a semiconductor die including an active surface;
a flat conductive plane disposed adjacent to the semiconductor die, wherein a surface of the flat conductive plane is coplanar with the active surface of the semiconductor die, and wherein the semiconductor die includes a first side oriented toward the flat conductive plane and a second side oriented away from the flat conductive plane; and
a conductive layer formed directly over the flat conductive plane and directly over the active surface of the semiconductor die, wherein the conductive layer includes,
a first conductive trace electrically coupling the semiconductor die to the flat conductive plane, and
a second conductive trace extending from the semiconductor die and over the flat conductive plane without physically contacting the flat conductive plane.

21. The semiconductor device of claim 20, wherein the flat conductive plane is disposed on an interconnect structure.

22. The semiconductor device of claim 21, wherein the interconnect structure includes a substrate and a plurality of conductive vias formed through the substrate with one of the conductive vias electrically connected to the flat conductive plane.

23. The semiconductor device of claim 20, wherein the flat conductive plane is disposed on a dummy die.

24. The semiconductor device of claim 20, further including an encapsulant deposited over the semiconductor die and the flat conductive plane.

25. The semiconductor device of claim 20, wherein the flat conductive plane is disposed outside a footprint of the semiconductor die.