

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
4 December 2003 (04.12.2003)

PCT

(10) International Publication Number
WO 03/100790 A1

(51) International Patent Classification⁷: **G11C 16/16**,
16/04, 11/56

(21) International Application Number: PCT/US03/12636

(22) International Filing Date: 22 April 2003 (22.04.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/155,767 24 May 2002 (24.05.2002) US

(71) Applicant: **ADVANCED MICRO DEVICES, INC.**
[US/US]; One AMD Place, Mail Stop 68, Sunnyvale, CA
94088-3453 (US).

(72) Inventors: **LE, Binh, Quang**; 1277 Crestpoint Drive,
San Jose, CA 95131 (US). **HAMILTON, Darlene**; 5824
Ponce Court, San Jose, CA 95120 (US). **TANPAIROJ,**
Kulachet; 948 Wing Place, Palo Alto, CA 94305 (US).

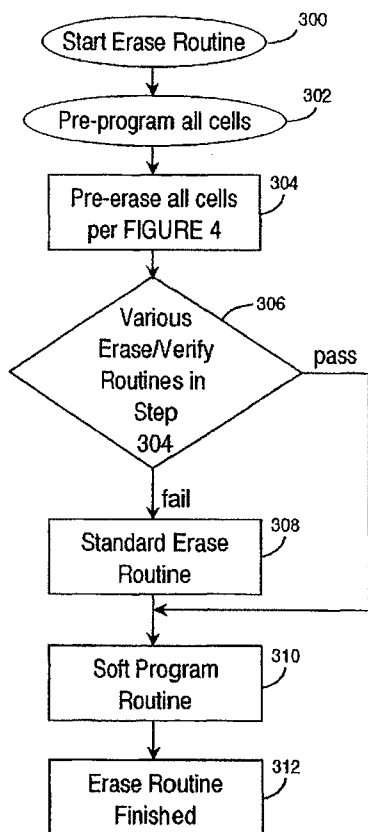
LIU, Zhizheng; 1319 Kingfisher Way #1, Sunnyvale, CA
94087 (US). **HE, Yi**; 3919 Riverbond Terrace, Fremont,
CA 94555 (US). **ZHENG, Wei**; 1180 Lochinvar Avenue,
#67, Sunnyvale, CA 94087 (US). **CHEN, Pau-Ling**;
12974 Arroyo De Arguello, Saratoga, CA 95070 (US).
VANBUSKIRK, Michael; 18653 Vessing Road, Saratoga,
CA 95070 (US).

(74) Agent: **COLLOPY, Daniel, R.**; Advanced Micro Devices,
Inc., One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-
3453 (US).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU,
AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ,
DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR,
HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR,
LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ,
NI, NO, NZ, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK,
SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU,
ZA, ZM, ZW.

[Continued on next page]

(54) Title: METHOD OF ERASING A FLASHING MEMORY USING A PRE-ERASING STEP



(57) Abstract: A method of erasing a sector of flash memory cells wherein a first set of preset pre-erase voltages is applied to the sector of flash memory cells (402). After the first set of preset pre-erase voltages is applied it is determined if another set of preset pre-erase voltages is to be applied to the sector of flash memory cells (410). If another set of preset pre-erase voltages is not to be applied, a standard erase routine is applied to the sector (411).

WO 03/100790 A1



(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.