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- 1 -

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CLOCK DRIVER APPARATUS WITH PROGRAMMABLE OUTPUT CHARACTERISTICS

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FIELD OF THE INVENTION

10 The present invention relates to clock drivers and clock trees and, more specifically, to providing clock drivers and clock trees with programmable output characteristics.

BACKGROUND OF THE INVENTION

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In application specific integrated circuits (ASICs) and in other integrated circuits a clock signal may be distributed to thousands and perhaps tens of thousands of "locations". This distribution is conventionally achieved using clock trees and a typical clock tree consists of a plurality of buffer drivers arranged in stages with each stage having more
20 outputs than inputs.

If a representative clock tree provides a 1:10 input to output ratio at each stage and has four stages, then the number of clock signal lines increases from 1 to 10, 10 to 100, 100 to 1,000 and 1,000 to 10,000 at stages 1-4, respectively. This staged increase in the
25 number of signal lines provides a like increase in the number of simultaneous or nearly simultaneous clock signal transitions (e.g., from positive to negative and vice versa). Since clock signal transitions are a source of electromagnetic interference (EMI), large numbers of simultaneous clock signal transitions produce an undesirably large amount of EMI. This problem is further exacerbated as semiconductor technologies advance.
30 Reduction in integrated circuit feature size increases the density of clock signal transitions

per unit area. Furthermore, faster operating speeds tend to increase a circuit's sensitivity to EMI and other parasitics.

SUMMARY OF THE INVENTION

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In accordance with the present invention, there is provided a clock driver circuit, comprising:

a first transistor unit having a first MOS transistor coupled between power and an output and a second MOS transistor coupled between said output and ground;

10 a second transistor unit having a third MOS transistor coupled between power and said output and a fourth MOS transistor coupled between said output and ground; and

a clock signal input coupled to each of said MOS transistors;

wherein the sized of the gate of at least one of said MOS transistors is different from that of the other MOS transistors.

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In another aspect, there is provided a clock signal distribution circuit for an integrated circuit, comprising:

a first stage clock signal driver circuit having a clock signal input and output;

a second stage circuit group including a plurality of second stage clock signal
20 driver circuits each having a clock signal input and output, the clock signal input of each of said second stage clock signal driver circuits being connected to the output of said first stage clock signal driver circuit, and

a plurality of third stage circuit groups each including a plurality of third stage clock signal driver circuits that each have a clock signal input and output, the input of
25 each of the third stage clock signal driver circuits of a given third stage circuit group being connected to the output of one of said second stage clock signal driver circuits;

wherein the clock signal driver circuits of said second and third stage each include a parallel arrangement of at least a first and a second transistor unit, said first transistor unit including a first MOS transistor coupled between power and an output and a second
30 MOS transistor coupled between said output and ground, and said second transistor unit

- 3 -

including a third MOS transistor coupled between power and said output and a fourth MOS transistor coupled between said output and ground.

The attainment of the foregoing and related advantages and features of the invention should be more readily apparent to those skilled in the art, after review of the following more detailed description of the invention taken together with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram of a clock tree in accordance with the present invention.

Fig. 2 is a schematic block diagram of a clock signal driver circuit in accordance with the present invention.

Fig. 3 is a schematic block diagram of selection logic 231 for use in circuit 100 of Fig. 2 in accordance with the present invention.

DETAILED DESCRIPTION

Referring to Fig. 1, a schematic block diagram of a clock tree in accordance with the present invention is shown. The embodiment of Fig. 1 illustrates a representative clock tree having four stages, though it should be recognized that the clock tree may have more or less stages without departing from the present invention.

Clock tree 5 includes a clock source 8 which is conventionally a crystal oscillator or the like. A clock signal output from source 8 is propagated over line 9 to a first stage (10) buffer driver 11 (hereinafter referred to as a "driver"). The output of driver 11 is delivered to a plurality of second stage (20) drivers, four of which are shown (21-24). While four are shown, it should be recognized that this number can be as large or as small as permitted by known fanout or load determining factors such as impedance, conductor

21 March 2002

- 4 -

length, etc. The outputs of the

second stage drivers are in turn coupled to the input or third stage (30) drivers 31-36 and the third stage drivers are similarly coupled to fourth stage (40) drivers 41-46. In the illustrated embodiment, clock signals output from the fourth stage are delivered to their destination (functional logic) that is indicated by loads 51-56. It should be recognized that the number of stages and the number of drivers within each stage is dependent upon the number of locations to which the clock signal need be delivered and the fanout ability of each driver, etc., as is generally known.

In accordance with the present invention, some or all of the drivers (11, 21-24, 31-36, 41-46) are configured such that they permit programmable shaping of their output clock signal. The drivers may be controlled individually, in sets (e.g., drivers 31-33, 34-36, 41-43 and 44-46 may each be considered a "set" of drivers), in stages or as otherwise desired by a circuit designer. It should be recognized that the provision of programmable clock signal shaping may be more critical in the latter stages of the clock tree (such as the third and fourth stages of Fig. 1) because the number of nearly simultaneous clock signal transitions is increased at these stages. It should also be recognized that staggering the timing or shape of the clock signals output from the second stage drivers 21-24 creates staggered clock signal transitions throughout clock tree 10.

The ability to program output clock signals is a function of the design of the drivers (as discussed in more detail below with reference to Fig. 2) and the delivery of appropriate control signals. While control signals may be delivered in many known manners (including tying inputs to a particular logic state, etc.), in a preferred embodiment, select lines 60 are provided that propagate signals from control logic 70. Control logic 70 preferably includes one

or more data registers and a processor that writes control/select bits to the data registers. The data registers hold the value of a clock driver selection signal as discussed below.

Referring to Fig. 2, a schematic block diagram of a clock signal driver circuit 100 in accordance with the present invention is shown. Each of the drivers 11, 21-24, 31-36, 5 and 41-46 may be configured to include driver circuit 100. It is not necessary to configure driver 11 with programmable output characteristics if it is the only first stage buffer from source 8. It is preferred, however, that the other drivers or sets or subsets thereof are configured to provide programmable output characteristics.

Fig. 2 illustrates that driver circuit 100 has a plurality of transistor units 10 comprising CMOS transistors 110,120,130. Appropriate combinational logic, such as an AND gate or the like (111,121,131), is coupled to the gate of the PMOS and NMOS transistors 112,122,132 and 113,123,133, respectively, to control current flow therethrough. An input clock signal is delivered online 105 to each of the AND gates. Another input to each of the AND gates is a select line such as one of the select lines 60 15 of Fig. 1. Each of the select lines 60 preferably includes a plurality of individual transistor control lines. Three control lines 161-163 are shown in Fig. 2. A three bit representative selection signal of "101" is indicated as being delivered by these lines. The value 101 (or other value delivered by the control lines) is stored, for example, in the data register of control logic 70.

20 The output of each CMOS transistor is coupled to a common output line to which load 150 is coupled. The circuit or other componentry driven by driver circuit 100 is represented generally by load 150. Each load has an appreciable capacitance associated therewith and this

capacitance is represented in phantom lines by capacitor 151.

While clock signals propagating through drivers are often illustrated as having a crisp square wave form, in reality these clock signals have rounded corners or, from another perspective, curved or sloping transitions. The rounded corners and curved transitions are a result, at least in part, of the time constant created by inherent or parasitic resistance in the clock signals current path and capacitance 151 in the load.

Circuit 100 permits selection of the value of resistance in the clock signal's current path (within the driver) and this selected value in combination with the capacitance of the load creates a time constant that determines the shape of the output clock signal transitions. The provision of selectable time constants permits a circuit designer to soften and/or separate clock signal transitions. The softened and/or spaced clock signal transitions result in significantly reduced EMI and related noise.

Referring more specifically to the embodiment of Fig. 2, select/control lines 161-163 permit a user to selectively enable CMOS transistors 110,120,130. Each enabled CMOS transistor effectively functions as a voltage divider with the necessary resistive components being provided primarily by the surface area dependent resistance value of the gate(s). Accordingly, if the three CMOS transistors have the same size gates (i.e., the same resistive values), then a designer may select between three possible resistive values, those values provided by enable one, two or three of the transistors. Alternatively, the CMOS transistors may be configured such that one or more have differently sized gates. For example, if each of transistors 110,120,130 have a different sized gate, then a designer may select from amongst seven possible resistive

values for circuit 100. These include the following enabled CMOS transistor scenarios (which are followed by their selection signal as propagated on lines 161-163 in parentheses): 110 (101), 120 (010), 130 (001), 110+120
5 (110), 110+130 (101), 120+130 (011) and 110+120+130 (111).

It should also be recognized that while the present invention is shown in Figs. 2-3 in a CMOS embodiment, it may also be implemented in an NMOS or PMOS setting, either using selectable NMOS or PMOS transistors arranged
10 generally as discussed above or selectable NMOS or PMOS transistors in combination with resistors formed in the semiconductor material.

Referring to Fig. 3, a schematic block diagram of selection logic 231 for use in circuit 100 of Fig. 2 in
15 accordance with the present invention is shown. Logic 231 essentially takes the place of any or all of the AND gates of circuit 100. In Fig. 3, logic 231 is described as though it replaces gate 131, though it may understandably also replace gates 111,121.

20 Logic 231 provides an inverter 241, a NAND gate 242 and a NOR gate 243. The input clock signal on line 205 is propagated to the NAND and NOR gates. The select signal is propagated via line 263 to the NOR gate and through inverter 241 to the NAND gate. Logic 231 permits CMOS
25 transistor 230 (analogous to CMOS transistor 130) to be tri-stated such that a signal may be driven into the clock signal output 250.

While the invention has been described in connection with specific embodiments thereof, it will be understood
30 that it is capable of further modification, and this application is intended to cover any variations, uses, or adaptations of the invention following, in general, the principles of the invention and including such departures from the present disclosure as come within known or
35 customary practice in the art to which the invention

pertains and as may be applied to the essential features hereinbefore set forth, and as fall within the scope of the invention and the limits of the appended claims.

CLAIMS

1. A clock driver circuit, comprising:
a first transistor unit having a first MOS transistor coupled between power and an
5 output and a second MOS transistor coupled between said output and ground;
a second transistor unit having a third MOS transistor coupled between power and
said output and a fourth MOS transistor coupled between said output and ground; and
a clock signal input coupled to each of said MOS transistors;
wherein the sized of the gate of at least one of said MOS transistors is different
10 from that of the other MOS transistors.
2. The clock driver circuit of claim 1, wherein the size of the gate of one of said
MOS transistors in said first transistor unit is different from the size of the gate of one of
said MOS transistors in said second transistor unit.
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3. The clock driver circuit of claim 1, further comprising enable storage logic that is
capable of holding a value for each of said transistor units that either enables or disables
that transistor unit depending on the value.
- 20 4. The clock driver circuit of claim 3, further comprising a third transistor unit
having a fifth MOS transistor coupled between power and said output and a sixth MOS
transistor coupled between said output and ground; and
wherein at least two of the gates of said first through sixth transistors have a size
that is different from the other transistors.
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5. The driver circuit of claim 4, further comprising control logic that programs said
enable storage logic with the enable or disable value of each of said transistor units.
6. The driver circuit of claim 5, wherein said input is configured to receive a clock
30 signal and said output fanouts to a plurality of at least four clock driver circuits that each

have at least two transistor units that each include at least two MOS transistors coupled like said first and second transistors.

7. The driver circuit of claim 1, further comprising tri-state logic coupled to at least
5 one of said transistor units.

8. A clock signal distribution circuit for an integrated circuit, comprising:
a first stage clock signal driver circuit having a clock signal input and output;
a second stage circuit group including a plurality of second stage clock signal
10 driver circuits each having a clock signal input and output, the clock signal input of each
of said second stage clock signal driver circuits being connected to the output of said first
stage clock signal driver circuit, and

a plurality of third stage circuit groups each including a plurality of third stage
clock signal driver circuits that each have a clock signal input and output, the input of
15 each of the third stage clock signal driver circuits of a given third stage circuit group
being connected to the output of one of said second stage clock signal driver circuits;
wherein the clock signal driver circuits of said second and third stage each include
a parallel arrangement of at least a first and a second transistor unit, said first transistor
unit including a first MOS transistor coupled between power and an output and a second
20 MOS transistor coupled between said output and ground, and said second transistor unit
including a third MOS transistor coupled between power and said output and a fourth
MOS transistor coupled between said output and ground.

9. The clock signal distribution circuit of claim 8, further includes programming logic
25 coupled to each of said transistor units that programs which of the transistor units are
enabled.

10. The clock signal distribution circuit of claim 8, wherein the size of the gate of at
least one of said MOS transistors in each driver circuit in said second and third stages is
30 different from that of one of the other MOS transistors in that same driver circuit.