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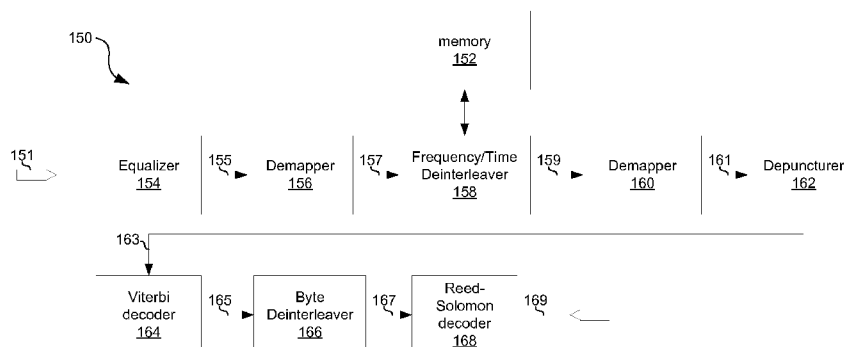


FIG. 1B

(57) Abstract: A plurality of data lines and a plurality of bit lines may be used to write to and/or read from an array of memory cells. A switching element may select among different mappings between the plurality of data lines and the plurality of bit lines. The array may, for example, consist of N memory cells, the plurality of bit lines may consist of N bit lines, and the plurality of data lines may consist of N data lines, where N is an integer greater than 1. For a write operation in which a data block is to be written to the array, a configuration of the switching element may be controlled based, at least in part, on how sensitive the data block is to a faulty memory cell among the array of memory cells.