Process Integration Scheme of SONOS Technology

Abstract

In an non-limiting example, we provide a substrate having a cell region, and non-cell regions. We form a tunneling dielectric layer, a charge storing layer, a top insulating layer (e.g., ONO), over the substrate. Then we form a conductive pad layer over the top insulating layer. We form isolation trenches in the pad layer, the charge storing layer and the tunneling dielectric layer and into the substrate. We form isolation regions in the isolation trenches. We remove the pad layer, charge storing layer and the tunneling dielectric layer in the non-cell regions. We form a gate layer over the pad layer and the substrate surface. We complete to form the memory (e.g., SONOS) device in the cell region and other devices in the non-cell regions of the substrate.

Fig. 8