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(71) Applicant: APPLIED MATERIALS, INC. [US/US]; 3050 Bowers Avenue, Santa Clara, CA 95054 (US).

(72) Inventor: PARIKH, Suketu, A.; 4624 Aviara Court, San Jose, CA 95135 (US).

(74) Agents: BERNADICOU, Michael, A. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

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(54) Title: TECHNIQUES FOR TRIPLE AND QUADRUPLE DAMASCENE FABRICATION

(57) Abstract

The present invention provides integrated circuit fabrication methods and devices wherein triple damascene structures are formed in five consecutive dielectric layers (312, 314, 316, 318 and 320) using two etching sequences. A first etching sequence comprising: depositing a first etch mask layer (322), on the fifth (top) layer (320), developing a power line trench pattern (324) and a via pattern (326) in the first mask layer, simultaneously etching the power line trench pattern (324) and the via pattern (326) through the top three dielectric layers (316, 318, 320), and removing the first etch mask layer. A second etching sequence including: depositing a second etch mask layer (330), on the fifth layer (320) and inside the power line trench (325) formed in the first etching sequence, developing a signal line pattern (332) overlaying the via pattern (327) in the second etch layer, etching the via pattern (327) through the second layer (312), and subsequently etching the via pattern (327) through the first layer (312) while simultaneously etching the signal line trench pattern (332) through the fifth layer (320). The etching sequences result in the formation of a power line trench (325) and a signal line trench (336) with an underlying via hole (340). These trenches and the via hole are simultaneously filled with a conductive material, such as a metal, to form a triple damascene structure including a power line (352) and a signal line (354) having an underlying via plug (356).

