



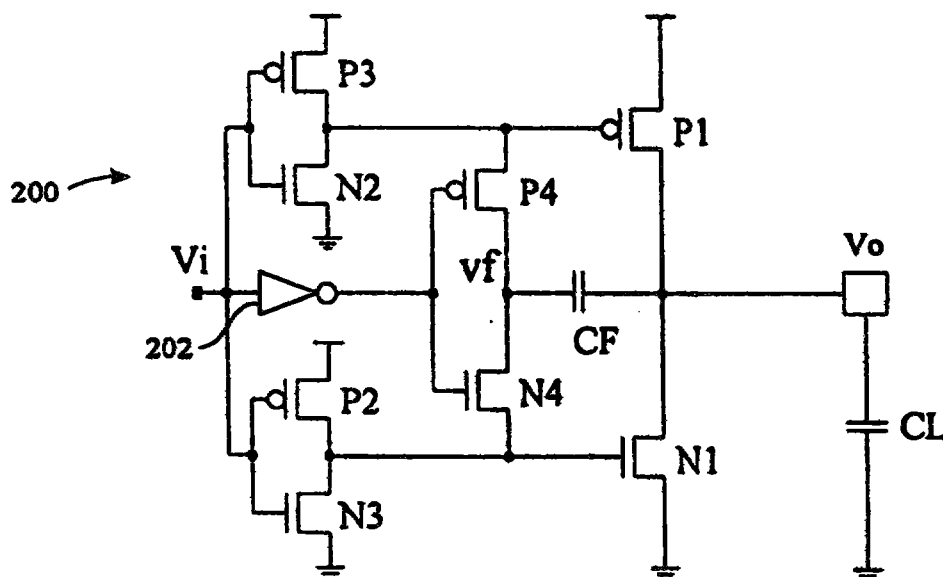
PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : H03K 3/00, H03B 1/00	A1	(11) International Publication Number: WO 99/26340 (43) International Publication Date: 27 May 1999 (27.05.99)
(21) International Application Number: PCT/US98/24394 (22) International Filing Date: 16 November 1998 (16.11.98) (30) Priority Data: 08/974,579 19 November 1997 (19.11.97) US (71) Applicant: ATMEL CORPORATION [US/US]; 2325 Orchard Parkway, San Jose, CA 95131 (US). (72) Inventor: GARCIA, Florent; 13, rue Grande Pujode, F-13530 Trets (FR). (74) Agent: SCHNECK, Thomas; Law Offices of Thomas Schneck, P.O. Box 2-E, San Jose, CA 95109-0005 (US).		(81) Designated States: CA, CN, JP, KP, KR, NO, SG, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published With international search report. With amended claims and statement.

(54) Title: ZERO-DELAY SLEW-RATE CONTROLLED OUTPUT BUFFER



(57) Abstract

An output buffer (100; 200) in accordance with the present invention exhibits a fixed output signal slew rate. The output signal behavior is independent of the capacitive load (CL) seen by the buffer. The circuit includes a capacitive feedback path from the output node to circuitry which drives the output transistors. In one embodiment, the feedback path comprises two capacitive elements (CFP, CFN), one which comes into play during a rising edge transition and the other which affects a falling edge transition. In a second embodiment, a single capacitive element (CF) is coupled to a switching circuit (P4, N4) for use during either a falling transition or a rising transition. The second embodiment provides precharging of the output transistor gates, and so improves response time.