

## REDUCED PARASITIC RESISTANCE AND CAPACITANCE FIELD EFFECT TRANSISTOR

### ABSTRACT

A field effect transistor and method for making the same is described wherein the field effect transistor incorporates a T- shaped gate (12) and source (22) and drain (24) contacts self-aligned with preexisting shallow junction regions. The present invention provides a low resistance gate electrode and self-aligned low resistance source/drain contacts suitable for submicron FET devices, and scalable to smaller device dimensions.

Fig.5

This Sheet Has Been Replaced



THIS SHEET HAS BEEN  
REPLACED