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| <b>PATENT</b>                                                                                                                                                                                                                                                                      |                                           |
| Docket No.: 5774.40 (GT2H-1)                                                                                                                                                                                                                                                       |                                           |
| EXPRESS MAIL LABEL NO.: <u>NB437525220</u>                                                                                                                                                                                                                                         | DATE OF DEPOSIT: <u>July 19, 1996</u>     |
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## COLUMN ADDRESS COUNTER WITH MINUS TWO SUBTRACTOR FOR ADDRESS COMPARE

### Background of the Invention

The present invention relates generally to semiconductor design technology, and more particularly to a method and apparatus for indicating the completion of a counter sequence.

Speed and timing constraints have always been important considerations in designing electronic systems. Most system designs must match the timing requirements of all the components used, yet still be optimized for high speed. As a result, many integrated circuits, or "chips," utilize a synchronous design. A synchronous chip is one in which components of the chip are connected to a common system clock ("CLK"). Synchronous chips have latches, registers and counters connected to inputs and outputs, all on a single monolithic chip. Furthermore, synchronous chips provide many benefits to system designers, such as fewer external logic chips and higher operation speed.

One example of a synchronous chip is a synchronous dynamic random access memory ("SDRAM") with an on-board address counter. Address counters are commonly used with processors that are capable of burst read or burst write operation. A burst operation is a method of transferring a



series of data from one device to another. For example, when a processor initiates a burst read operation to an SDRAM, it provides a base address to denote a memory location in the SDRAM from which a first data is to be read. The processor then expects to read data one or more memory locations in the SDRAM according to a predetermined burst sequence.

Because the burst sequence has been predetermined, once the first memory location is accessed, counters that are separate from the processor are used to anticipate the next memory locations to be accessed. In so doing, operation of the SDRAM is improved because the counters can quickly generate an address for the next memory location to be accessed, and can initiate the access to that memory location next at an early time.

As processor operation speed, or frequency, has increased, the corresponding speed requirements for the address counters has increased. Therefore, in order to improve operation, address counters have been incorporated onto the SDRAMs themselves, thereby reducing any propagation delays resulting from discrete counters and SDRAMs. However, processor frequency has continued to increase, and simply including a conventional counter inside the SDRAM is not sufficient to meet the strict timing requirements of many modern processors, as described below.

Fig. 1 is a block diagram of a conventional counter, which is designated generally by a reference numeral 10. The counter 10 is incorporated into a SDRAM (not shown). The counter 10 receives an external address from an external address bus XADD. It is understood that supplying an address to a memory device is well known in the art, and will not be further described.

It is a goal of the counter 10 to produce internal addresses on the internal address bus IADD, based upon the external address, in a predetermined burst sequence. Although bursts can be of many different



lengths, such as one, two, four, eight or sixteen address locations, an exemplary burst sequence for two addresses A1:A0 of a 32 bit address A31:A0 is:

|                      |        |     |     |
|----------------------|--------|-----|-----|
| External Address     | A31:A2 | A1  | A0  |
| First Burst Address  | A31:A2 | A1  | A0\ |
| Second Burst Address | A31:A2 | A1\ | A0  |
| Third Burst Address  | A31:A2 | A1\ | A0\ |

(note: the symbol "\ " denotes an inverted address)

For the remaining description, the exemplary burst sequence shown above will be used. However, it is understood that other burst sequences and lengths may be used. In addition, it is a goal of the counter 10 to produce an end-of-burst signal WRAPDN, to indicate that the burst sequence is complete. The WRAPDN signal must also meet certain processor-defined set-up and hold times.

The counter 10 includes three address registers 12, 14, 16, an incrementor 20, a subtractor 18, a comparator 22, and a burst sequencer 24. Each of the registers 12, 14, 16 is synchronized by a K signal, which is driven by a clock circuit 26. The K signal is responsive to three control signals: LOAD, CLK and COUNTUP. The LOAD signal indicates when the address bus XADD contains a valid external address. The CLK signal is the system clock, as described above. The COUNTUP signal indicates when, during a burst sequence, the next memory location of the burst sequence may be accessed.

The burst sequencer 24 is programmable for different burst sequences. Using the exemplary burst sequence described above, the burst sequencer 24 simply passes signals straight through without altering them. However, the burst sequencer 24 can be programmed to support different burst sequences.



In operation, the LOAD signal allows the external address on the external address bus XADD to be loaded into the address registers 12, 14, 16. The address register 16 drives the external address on the internal address bus IADD as the first address of the predetermined burst sequence.

The address register 14 drives an intermediate address A1, which is equal to the external address, to the subtractor 18. The subtractor 18 subtracts one from the intermediate address A1 to produce an intermediate address A2, which is equal to the third internal address of the predetermined burst sequence, as shown above.

Meanwhile, the address register 12 drives an intermediate address A3, which is initially equal to the external address, to the incrementor 20. The incrementor 20 adds one to the intermediate address A3 to produce an intermediate address A4, which is equal to the first burst address of the predetermined burst sequence, as shown above. The intermediate address A4 is supplied to the burst sequencer 24, which produces an intermediate address A5 according to the predetermined burst sequence. The intermediate address A5 is then supplied to the address register 16. The address register 16 thereby updates the internal address on the internal address bus IADD to the next address of the predetermined burst sequence.

The intermediate address A4 is also looped back to the address register 12 in order to calculate the next burst address. Furthermore, the intermediate address A4 is supplied to the comparator 22, where it is compared with the intermediate address A2. In this way, once the intermediate address A4 is equal to the third burst address (which is the last address of the predetermined burst sequence), the comparator 22 can assert the WRAPDN signal.

Fig. 2 is a timing diagram for the conventional counter circuit of Fig. 1. The external address, first burst address, second burst address and third



burst address are denoted by the reference numerals B0, B1, B2, and B3, respectively.

Of particular importance is the waveform for the WRAPDN signal. The WRAPDN signal is asserted at a time 32, which is determined by a propagation delay 33. The propagation delay 33 is the sum of a first delay 34 and a second delay 36. The first delay 34 is due to the propagation delay of the incrementor 20 when driving the burst address B3. The incrementor 20 drives the burst address B3 on the intermediate address A4 after the intermediate address A3 is equal to the burst address B2. The second delay 36 is a high-going delay caused by propagation through the comparator 22.

Likewise, the WRAPDN signal is de-asserted at a time 38, which is determined by a propagation delay 39. The propagation delay 39 equals a sum of a hold time delay 40 of the incrementor 20 plus a low-going delay 42 caused by propagation through comparator 22.

The delays 33 and 39 create timing problems for the conventional counter 10. For the sake of example, the frequency of the clock signal CLK will be 100 mega-hertz ("MHz"), which provides a period T of 10 nano-seconds ("ns"). A typical time for the delay 34 is 8ns and for the delay 36 is 2ns. As a result, the cumulative delay 33 for the assertion of the WRAPDN signal is 10ns (8ns + 2ns), or one clock period. Such a delay is too long to meet the set-up time requirements of many conventional processors. As a result, a clock period is wasted while waiting for the assertion of the WRAPDN signal. It would be advantageous if the WRAPDN signal was asserted early enough to save the wasted clock period.

### Summary of the Invention

The present invention, accordingly, is a method and circuit for providing a burst address counter with a fast burst-done signal. In a preferred embodiment, a synchronous memory device includes a counter for



producing a sequence of burst addresses, based on an external address. In addition, the counter drives the burst-done signal to indicate completion of the burst sequence. The counter includes a register for receiving the external address, an incrementor for incrementing the external address to produce the next address of the sequence of burst addresses, a minus-two subtractor for determining a second-to-last burst address of the burst sequence, and a comparator.

By utilizing the minus-two subtractor, the comparator can determine the end of the burst sequence earlier than conventional counters. This is because the minus-two subtractor determines the next-to-last address of the sequence, which allows the comparator to start asserting the burst-done signal at an earlier time.

A technical advantage achieved with the present invention is that the burst-done signal is asserted early so that timing requirements of high speed processor systems may be met.

#### Brief Description of the Drawings

Fig. 1 is a block diagram of a conventional counter.

Fig. 2 is a timing diagram of the conventional counter of Fig. 1.

Fig. 3 is a block diagram of a 64 Mbit SDRAM embodying features of the present invention.

Fig. 4 is a block diagram of an improved counter for the 64 Mbit SDRAM of Fig. 4.

Fig. 5 is a timing diagram of the improved counter of Fig. 4, illustrating the features of the present invention.

Fig. 6 is a timing diagram of a burst operation, illustrating the feature of the present invention.

Fig. 7 is a diagram for an explanation of the burst operation of Fig. 6.

Fig. 8 is a diagram of a carry generation circuit included in an address register and a counter of Fig. 4.

Fig. 9 is a diagram of control registers included in the carry generation circuit of Fig. 8.



**Detailed Description of the Preferred Embodiment**

As described above, Figs. 1 and 2 illustrate a conventional counter and associated timing diagram.

Referring to Fig. 3, the reference numeral 100 designates a synchronous memory device embodying features of the present invention. While in a preferred embodiment of the invention, the device 100 is a 64 Mbit synchronous dynamic random access memory ("SDRAM"), it should be understood that the present invention is not limited to use with a SDRAM, but may be used in conjunction with any circuit device operating at high speeds and utilizing a counter.

The device 100 receives a positive external power supply (VDD) and a negative external power supply (VSS) through input pads 102 and 104, respectively. The device 100 transmits and receives data input-outputs (I/Os) through I/O pads 106a, 106b, 106c, and 106d. Furthermore, the device 100 comprises a plurality of input buffers, output buffers and other circuits, referenced generally by an I/O circuits group 108. The I/O circuits group 108 and the input pads 106a-106d are conventional for most SDRAMs, and will not be discussed in greater detail.

The device 100 receives an external address through address pads 110a, 110b, 110c, and 110d, and control signals RAS\, CAS\, CLK, CKE, WE\ and DQM through pads 112a, 112b, 112c, 112d, 112e, and 112f respectively. Each of the signals RAS\, CAS\, CLK, CKE, WE\ and DQM are conventional, and some of which are used to derive internal signals LOAD and COUNTUP. The LOAD and COUNTUP signals are also conventional internal signals as described above, with reference to Fig. 1. The device 100 also drives an internal control signal WRAPDN'. In the preferred embodiment, many more address and control signal pads may exist, but their functionality can be represented by the pads 110a-110d and 112a-112f.



The device 100 also contains a plurality of address buffers and decoders, represented generally by the address buffer group 114, the row address decoder group 116 and the column address decoder group 118. The address buffer group 114 and decoder groups 116 and 118 are conventional for most DRAMs and SDRAMs, and will not be discussed in greater detail.

The device 100 contains 64 Meg (1 meg equals 1,048,576) of memory cells. The memory cells are grouped into four equal-sized banks 120, 122, 124, 126, each having an upper and lower portion represented by the suffix "u" or "l", respectively. The memory cells are conventional, and utilize many different signal lines, amplifier circuits and decoder circuits. Because the banks 120-126 contain memory cells conventional for most 64 Mbit DRAMs, their functionality will not be discussed in greater detail.

The device 100 contains a counter 130. The counter 130 is an improvement of the conventional counter 10 (Fig. 1); therefore, the circuits and signals of the improved counter 130 that are identical to those of the conventional counter 10 will be designated by the same reference name or numeral, and any changed, modified or improved circuits and signals will be designated by a new name or numeral.

The counter 130 is connected to the address buffer 114 through an external address bus XADD. Likewise, the counter 130 is connected to the column decoder 118 through an internal address bus IADD. The counter 130 is also connected to the power supplies VDD and VSS.

The counter 130 receives as inputs the external address from the external address bus XADD, and the external and internal control signals CLK, LOAD, and COUNTUP. The counter 130 drives internal addresses on the internal address bus IADD that simulate a predetermined burst sequence. Although bursts can be of many different lengths, such as one,



two, four, eight or sixteen address locations, for the sake of example, the predetermined burst sequence is:

|                      |        |     |     |
|----------------------|--------|-----|-----|
| External Address     | A31:A2 | A1  | A0  |
| First Burst Address  | A31:A2 | A1  | A0\ |
| Second Burst Address | A31:A2 | A1\ | A0  |
| Third Burst Address  | A31:A2 | A1\ | A0\ |

Furthermore, the counter 130 drives the internal WRAPDN' signal.

Referring to Fig. 4, the counter 130 includes three address registers 12, 14, 16, an incrementor 20, a comparator 22, and a burst sequencer 24. Each of these circuits are similar to those used in the conventional counter 10 of Fig. 1. Each of the registers 12, 14, 16 is synchronized by a K signal, which is driven by a clock circuit 26 and derived from the three control signals LOAD, CLK and COUNTUP.

The counter 130 also includes a minus two subtractor 138. The minus-two subtractor 138 is used to determine the second-to-last address of the predetermined burst sequence. Using the predetermined burst sequence described above, the minus-two subtractor 138 may simply invert only one of the address lines (A1) of the external address.

In operation, the LOAD signal allows the external address from the external address bus XADD to be loaded into the address registers 12, 14, 16. The address register 16 drives the external address on the internal address bus IADD as the first address of the predetermined burst sequence.

The address register 14 drives an intermediate address A1, which is equal to the external address, to the minus two subtractor 138. The subtractor 138 subtracts two from the intermediate address A1 to produce an intermediate address A2', which is equal to the second internal address of the predetermined burst sequence shown above.

Meanwhile, the address register 12 drives an intermediate address A3, which is initially equal to the external address, to the incrementor 20.



The incrementor 20 adds one to the intermediate address A3 to produce an intermediate address A4, which is equal to the first burst address of the predetermined burst sequence, as shown above. The intermediate address A4 is supplied to the burst sequencer 24, which produces an intermediate address A5. The intermediate address A5 is then supplied to the address register 16 to drive the internal addresses on the internal address bus IADD. The address register 16 updates the internal addresses. The intermediate address A4 is also looped back to the address register 12 in order to calculate the next burst address.

The intermediate address A3 is also supplied to the comparator 22, where it is compared with the intermediate address A2'. In this way, once the intermediate address A3 is equal to the second burst address, the comparator 22 can begin to assert the WRAPDN' signal.

The burst sequencer 24 is programmable for different burst sequences. Using the exemplary burst sequence described above, the burst sequencer 24 simply passes signals straight through without altering them. The burst sequencer 24 is also connected to the intermediate address A1 and a BURST signal (not shown). As a result, the BURST signal can selectively enable the burst sequencer 24 to produce a different burst sequence by exclusive or-ing the intermediate address A1 with the intermediate address A4, or by performing other conventional operations.

Referring to Fig. 5, the external address, first burst address, second burst address and third burst address are denoted by the reference numerals B0, B1, B2, and B3, respectively. Of particular importance is the waveform for the WRAPDN' signal. The WRAPDN' signal of Fig. 5 is improved over the WRAPDN signal of Fig. 2. The WRAPDN' signal is asserted at a time 140, which is determined by a high-going delay 36 caused by the comparator 22 once the intermediate address A2 equals the second burst address B2. Likewise, the WRAPDN signal is de-asserted at a time



142, which is determined by a low-going delay 42 caused by the comparator 22, once the intermediate address A2 equals the third burst address B3.

To illustrate some of the benefits of the present invention, the same timing example used with conventional Fig. 2 will be applied to Fig. 5. The frequency of the clock signal CLK is 100MHz, which provides a period T of 10ns. A typical time for the delay 36 is 2ns. Note, however, that there is no delay 34 from generating the burst address B3 from the intermediate address A3, as exists with the conventional counter 10. As a result, the WRAPDN' signal of the present invention is asserted 8ns earlier than the WRAPDN signal of conventional Fig. 2.

Although illustrative embodiments of the present invention have been shown and described, a latitude of modification, change and substitution is intended in the foregoing disclosure, and in certain instances, some features of the invention will be employed without a corresponding use of other features. Furthermore, additional buffers, drivers, delay circuits and other circuits may be added to the illustrative embodiment without altering the scope of the invention. Accordingly, it is appropriate that the appended claims be construed broadly and in a manner consistent with the scope of the invention.

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~~(TEXT 2)~~

Figure 6 shows a timing diagram illustrating the timings of the burst operation, for example, the burst read operation, based on the burst sequence which is a feature of this invention. After the first address is selected, successive 8-bit data can be obtained in a burst mode, with a burst length of 8 cycles and a CAS latency of 2 cycles. Constitutional elements for implementing the burst read operation are shown in Figure 7.

Figure 7 shows a plurality of memory cells MC arranged in a matrix at intersections of word lines and bit lines; sense amplifiers SA corresponding to the memory cells MC; a pair of selection MOS transistors ST connecting the sense amplifiers SA to the I/O lines; a main amplifier MA connected to the I/O lines; and an output latch circuit OL for latching and outputting the output of the main amplifier MA. Each pair of the selection MOS transistors ST is connected through a YS line to a column decoder CD, which receives a column address from a column counter CC.

Only by disconnecting the I/O lines from the output latch circuit OL after the output latch circuit OL provided to the common I/O line has latched the



data read out of memory cells MC through bit lines, sense amplifier SA, I/O lines and the main amplifier MA, it is possible to perform other operations such as precharging the I/O lines having a large load

5 capacitance while the latched data are being taken out.

The column counter CC and the column decoder CD shown in Figure 7 correspond to the counter 130 and the column decoder 118 of Figure 3, respectively. The  
10 memory cells MC, sense amplifiers SA and selection MOS transistors ST can be included in the banks 120, 122, 124, 126, and the main amplifier MA and the output latch circuit OL can be included in the I/O circuit  
108.

15 In the burst read operation, as shown in the timing diagram of Figure 6, the memory array takes in a command and an address at the leading edge of the clock CLK, in a synchronous operation mode using the clock CLK. According to an active (ACTV) command, the  
20 memory array takes in a row address (RA) to select the corresponding word line. The cell signals read into bit lines—eight-bit lines in this case—are amplified by the sense amplifier SA. According to a read (READ) command issued two cycles after the active command,  
25 the memory array takes in a column address (CA), reads



the amplified signals by means of a pair of selection MOS transistors ST from the corresponding bit lines onto the I/O line, and outputs the amplified signals to the external circuit in synchronism with the clock  
5 CLK.

At this time, the column counter CC can instantly generate the address of the next memory cell MC to be accessed. Hence, when a column address is specified by the column counter CC, the YS lines corresponding  
10 to the column addresses (CA to CA+7) from the specified address are selected successively and the selection MOS transistors ST are driven, thereby outputting 8-bit signals successively from the corresponding eight-bit lines onto the I/O lines.  
15 After being amplified by the main amplifier MA, the outputs (MO1-MO8) are latched by the output latch circuit OL, which then outputs the data (OUT1-OUT8) to the external circuit in synchronism with the clock CLK.

20 The data outputting in this burst read operation is performed as follows. After a row address is taken in according to the active command, a column address is taken in according to the read command, two cycles after the column address is taken in the data from the  
25 OUT1 to the OUT8 are outputted in order in synchronism

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with the clocks CLK, thus all the data from the OUT1 to the OUT8 being outputted in eight cycles successively.

Here we have described the operation in which the  
5 burst length is 8 cycles and the CAS latency is 2  
cycles. The data output operation in which the CAS  
latency is three cycles also includes basically the  
same internal operation except that the number of  
cycles from the address specification to the data  
10 output differs. For other burst lengths, too, it is  
possible to successively output data of desired bits  
such as 2, 4, 16, 256 or 1024, in a desired number of  
cycles such as 1, 2, 4 or full.

Figure 8 illustrates a carry generation circuit  
15 included, for example, in the address register 12 and  
adder 20 of the counter 130 of Figure 4. The carry  
generation circuit is, for instance, a 10-bit parallel  
adder of column address (CA) = (Y9, Y8, ..., Y0) with  
a two-stage carry-lock-ahead adder circuit  
20 configuration for improving the addition speed by  
performing addition of the addend and the augend for  
each digit to find a partial sum, at the same time  
independently performing carry calculation for all  
digits, and then adding the partial sum and the carry.

25 This carry generation circuit comprises 10



control registers CTR0-CTR9 for calculating partial sums and a gate circuit including HAND gates, NOR gates and inverters that is connected to the input stages of these control registers and performs carry  
5 calculation for all digits. The carry generation circuit is so designed that the carry outputs (C) from the control registers for the low-order digits are reflected on the carry inputs (CR) of all control registers for the higher-order digits. From the  
10 outputs (S) of the control registers CTR0-CTR9 is produced 10-bit data (Y0-Y9) that corresponds to the intermediate address A4 shown in Figure 4.

For example, the carry input of the control register CTR0 for bit 0 is fixed to a high level, and  
15 its carry output is taken into the carry input of the control register CTR1 for bit 1. At the same time the carry output of the control register CTR0 is also taken into one of carry inputs of a 2-input NAND gate connected to the control register CTR2 for bit 2 and  
20 into one of carry inputs of a 3-input NAND gate connected to the control register CTR3 for bit 3. The outputs of these NAND gates are fed through the inverters to the inputs of the control registers CTR2, CTR3 of bit 2 and bit 3.

25 Further, for the control registers CTR4-CTR6 for



bit 4 to bit 6, too, the carry inputs of low-order bits are fed to the control registers for higher-order bits through an inverter and a 2-input NOR gate, through a 2-input NAND gate and a 2-input NOR gate, and through a 3-input NAND gate and a 2-input NOR gate, respectively. Similarly, for the control registers CTR7-CTR9 for bit 7 to bit 9, the carry inputs can be taken into the control registers through an inverter and a 3-input NOR gate, and through a 2-input NAND gate and a 3-input NOR gate, through 3-input NAND gate and 3-input NOR gate, respectively.

In addition to the carry input (CR) signals, the control registers CTR0-CTR9 receive control signals such as CUP, CASP and INTEL, and address signals, none of these signals shown. Details of these signals will be described later referring to Figure 9 illustrating the internal logic configuration of the control registers CTR0-CTR9.

As shown in Figure 9, the control registers of Figure 8 can each be made a so-called binary counter in the form of a loop feedback circuit comprising logic gates such as a plurality of clocked inverters CIV1-CIV4, a plurality of inverters IV1-IV4 and a NAND gate, and a transfer CMOS transistor TT. The clocked inverters CIV1-CIV4 and inverters IV1-IV4 are made up



of CMOS transistors or a combination of PMOS transistors and NMOS transistors. These have conventionally been used and their explanation will not be given.

5        Each of these control registers comprises a clocked inverter CIV1 which is controlled by control signals CUP\, CUP and receives a loop feedback signal; a transfer CMOS transistor TT which is connected to the clocked inverter CIV1 via an inverter IV1 and  
10       whose gate is controlled by a control signal CUP; a clocked inverter CIV2 connected to the transfer CMOS transistor TT via an inverter IV2 and controlled by control signals CR\, CR; a clocked inverter CIV3 connected in parallel with the inverter IV2 and the  
15       clocked inverter CIV2 and controlled by control signals CR, CR\; a clocked inverter CIV4 connected to a connecting node between the transfer CMOS transistor TT and the inverter IV2 and controlled by control signals CASP\, CASP; and a NAND gate connected to the  
20       clocked inverter CIV4 and fed with an address signal ADD and a control signal INTEL. Statically, the inverters IV1, IV2 are connected to antiparallellly connected inverters IV3, IV4, to retain electric charge by the floating of clocked inverters.

25       The control registers take in the following



control signals. The control signals CUP, CUP\ are a  
COUNTUP signal of Figure 5 and its inverted signal;  
the control signals CR, CR\ are a signal carried up  
from a lower-order bit control register and its  
5 inverted signal; the control signal CASP, CASP\ are a  
LOAD signal of Figure 5 and its inverted signal; and  
the control signal INTEL is a control signal for  
changing the burst mode. The address signal ADD  
corresponds to an external address inputted through  
10 the external address bus XADD shown in Figure 5.

The control register operates as follows. First,  
in the initial setting of address, the control  
register controls the clocked inverter CIV4 according  
to the CASP signal to take in the address signal ADD  
15 fed to the NAND gate. This address is the first  
address of the burst sequence. The second address  
next to the first address is generated by controlling  
the clocked inverter CIV1 and the transfer CMOS  
transistor TT by the CUP signal to count up the first  
20 address. In such a way, the address before being fed  
back in loop is counted up successively to the next  
address of the burst sequence.

When the address is counted up to the last  
address of the burst sequence, the CUP signal is  
25 stopped. That is, the intermediate addresses of the

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burst sequence are fed to the comparator 22 of Figure 4 and, when it becomes equal to the last burst address of the predetermined burst sequence, the comparator 22 generates a WRAPDN' signal for terminating the count-  
5 up burst sequence.

When, for example, the control register receives a high-level carry signal CR from a lower-order bit control register, the control register inverts the received carry signal CR and outputs the inverted  
10 signal to higher-order bit control registers because the control register operates through a 3-stage inverter comprising a clocked inverter CIV1, an inverter IV1 and a clocked inverter CIV3. When the control register receives a low-level carry signal CR,  
15 it operates through a four-stage inverter comprising a clocked inverter CIV1, an inverter IV1, an inverter IV2 and a clocked inverter CIV2, and thus outputs the carry signal at it is to the higher-order bit control registers.

20 As described above, each control register can output data Y0 (Y1-Y9) corresponding to each bit as a burst sequence address and reflect the carry signal from a lower-order bit control register on all higher-order bit control registers.

25 Here in the burst sequence, delay is a critical



problem. The logic configuration of the address register 12 and adder 20 in the counter 130 of Figure 4 has been explained in detail. The address register 14 and the minus-2 subtractor 138, too, have a carry  
5 generation circuit as shown in Figure 8 and 9 and have the basically similar logic configuration, so detailed explanation will not be given.

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~~PROVISIONAL PATENT~~  
~~Docket No.: 5774.40 (GT2H-1)~~

## Claims

What is claimed is:

1           1.     A counter for producing a sequence of burst addresses from an  
2 external address and for producing a burst-done signal to indicate  
3 completion of the burst sequence, the counter comprising:

4                 a register for receiving the external address;

5                 a first circuit for incrementing the external address to produce  
6 a next address of the sequence of burst addresses;

7                 a second circuit for determining a second-to-last burst address  
8 of the sequence of burst addresses;

9                 a third circuit for determining if the next address equals the  
10 second-to-last address and for asserting the burst-done signal in  
11 response thereto.

1           2.     The counter of claim 1 wherein the first circuit is an  
2 incrementor circuit.

1           3.     The counter of claim 1 wherein the second circuit is a minus-  
2 two subtractor circuit.

1           4.     The counter of claim 1 wherein the third circuit is a  
2 comparator.

1           5.     The counter of claim 1 wherein the first circuit comprises a  
2 burst sequencer so that the sequence of burst addresses is programmable.

1           6.     A synchronous memory device comprising a plurality of  
2 memory cell locations, a plurality of address pads for receiving an external





~~PROVISIONAL PATENT~~  
~~Docket No. 5774.40 (GT2H-1)~~

3 address, and a counter for producing a plurality of internal addresses  
4 according to a predetermined sequence, the counter comprising:

5 a first circuit for advancing the external address to produce a  
6 next address of the predetermined sequence;

7 a second circuit for determining a second-to-last address of the  
8 sequence;

9 a third circuit for determining if the next address equals the  
10 second-to-last address and for asserting a burst-done signal in  
11 response thereto.

1 7. The synchronous memory device of claim 6 wherein the first  
2 circuit of the counter is an incrementor circuit.

1 8. The synchronous memory device of claim 6 wherein the second  
2 circuit of the counter is a minus-two subtractor circuit.

1 9. The synchronous memory device of claim 6 wherein the third  
2 circuit of the counter is a comparator.

1 10. The synchronous memory device of claim 6 wherein the first  
2 circuit of the counter comprises a burst sequencer so that the sequence of  
3 burst addresses is programmable.

1 11. A method for providing a sequence of burst addresses based  
2 upon an external address, the method comprising the steps of:

3 (a) receiving the external address into a register;

4 (b) supplying the address received into the register to a  
5 sequencing circuit;





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6 (c) sequencing the address supplied to the sequencing circuit to  
7 produce a next address of the sequence;

8 (d) receiving the next address into the register;

9 (e) comparing the address received into the register with a  
10 reference address for determining when the sequence is complete.

1 12. The method of claim 11 further comprising the steps of:  
2 if the sequence is not complete, repeating the steps of (b), (c),  
3 (d), and (e);  
4 if the sequence is complete, asserting a burst-done signal.

1 13. The method of claim 11 further comprising the step of:  
2 (f) driving the address received into the register to a memory  
3 circuit.

1 14. The method of claim 11 wherein the reference address is  
2 determined from the external address.

1 15. The method of claim 11 wherein the reference address is  
2 determined by subtracting two from the external address.

1 16. The method of claim 11 wherein the reference address is  
2 determined by inverting part of the external address.

1 17. The method of claim 11 wherein the sequencing is done by an  
2 incrementor.

1 18. The method of claim 11 wherein the sequencing is  
programmable to different burst sequences.





~~ADDITIONAL CLAIMS~~

19. A semiconductor memory comprising:

a memory array including a plurality of bit line pairs, a plurality of word lines crossing the bit line pairs, a plurality of memory cells, and a plurality of sense amplifier circuits connected to the bit line pairs;

a common data line pair for the plurality of the bit line pairs;

10 a switch circuit selectively connecting a predetermined bit line pair of the plurality of the bit line pairs to the common data line pair;

an adder circuit which outputs continuous addresses;

15 an address holding circuit which holds the output address from the adder circuit as the input address of the adder circuit;

a subtracter circuit which forms an address before the last address of the continuous addresses on the basis of the first address of the continuous addresses;

20 a comparator circuit which receives the input address of the adder circuit and the output address of the subtracter circuit; and

25 a control circuit which controls the switch

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circuit based on the continuous addresses;

wherein the operation of the adder circuit is stopped by an agreement detection signal from the comparator circuit.

5        20. A semiconductor memory according to claim 19, wherein the subtracter circuit is a circuit that subtracts two from the first address.

21. A semiconductor memory according to claim 20, wherein the first address is an external address  
10 and the initial value of the address holding circuit is the first address.

22. A semiconductor memory according to claim 21, further comprising

an internal clock generation circuit which  
15 generates an internal clock signal based on an external clock signal

wherein the adder circuit operates in synchronism with the internal clock signal.

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