CLAIMS

What is claimed is:

1. A method of operating a ferroelectric memory cell, comprising:

applying a positive voltage to a ferroelectric capacitor of the ferroelectric memory cell, wherein the ferroelectric capacitor is in electronic communication with a digit line;

determining that a rate of change of a voltage of the digit line has reached a threshold in response to the positive voltage being applied; and

applying a negative voltage to the ferroelectric capacitor after the voltage of the digit line reaches the threshold.

2. The method of claim **1**, further comprising:

comparing the voltage of the digit line to a ground reference after the negative voltage is applied.

3. The method of claim **2**, further comprising:

determining a logic value of the ferroelectric memory cell based at least in part on the comparison of the voltage of the digit line to the ground reference.

4. The method of claim **1**, wherein a magnitude of the negative voltage applied to the ferroelectric capacitor is based at least in part on the threshold.

5. The method of claim **1**, further comprising:

determining that the voltage of the digit line has reached a second threshold based at least in part on determining that the positive voltage has been applied for a predetermined duration.

6. The method of claim **5**, wherein the predetermined duration is based at least in part on at least one of:

a characteristic of the ferroelectric capacitor, a characteristic of the digit line, a timing associated with reading or writing to the ferroelectric memory cell, or any combination thereof.

7. The method of claim **1**, further comprising:

determining that the voltage of the digit line has reached a second threshold based at least in part on determining that the voltage of the digit line has reached a threshold voltage.

8. The method of claim **1**, wherein applying the positive voltage to the ferroelectric capacitor comprises:

virtually grounding the digit line;

applying the positive voltage to a plate line in electronic communication with the ferroelectric capacitor; and

applying a second voltage to a word line in electronic communication with the ferroelectric capacitor.

9. The method of claim **1**, wherein applying the negative voltage to the ferroelectric capacitor comprises:

applying the negative voltage to a plate line in electronic communication with the ferroelectric capacitor.

10. The method of claim **1**, wherein determining that the rate of change of the voltage of the digit line comprises determining that the rate of change is less than 10 mV/ns.

11. The method of claim **1**, wherein determining that the rate of change of the voltage of the digit line comprises determining that the voltage of the digit line is within a percent range of an expected settling voltage.

12. An electronic memory apparatus, comprising:

a ferroelectric memory cell that comprises a ferroelectric capacitor in electronic communication with a digit line; and

a controller in electronic communication with the ferroelectric memory cell and operable to:

connect a positive voltage source to the ferroelectric capacitor; and

determine that a rate of change of a voltage of the digit line has reached a threshold;

connect a negative voltage source to the ferroelectric capacitor after the voltage of the digit line reaches the threshold.

13. The electronic memory apparatus of claim **12**, wherein the controller is operable to:

compare the voltage of the digit line to a ground reference after a negative voltage is applied to the ferroelectric capacitor.

14. The electronic memory apparatus of claim **13**, wherein the controller is operable to:

determine a logic value of the ferroelectric memory cell based at least in part on a comparison of the voltage of the digit line to the ground reference.

15. The electronic memory apparatus of claim **12**, wherein the controller is operable to:

determine that a voltage of the digit line has reached a second threshold in response to a positive voltage applied to the ferroelectric capacitor.

16. The electronic memory apparatus of claim **15**, wherein the controller is operable to:

determine that a voltage of the positive voltage source has been applied to the ferroelectric capacitor for a predetermined duration; and

determine that the voltage of the digit line has reached the second threshold based at least in part on determining that the voltage of the positive voltage source has been applied for the predetermined duration.

17. The electronic memory apparatus of claim **16**, wherein the predetermined duration is based at least in part on at least one of:

a characteristic of the ferroelectric capacitor, a characteristic of the digit line, a timing associated with reading or writing to the ferroelectric memory cell, or any combination thereof.

18. The electronic memory apparatus of claim **12**, further comprising:

a plate line in electronic communication with the ferroelectric capacitor, wherein the controller is operable to:

applying a positive voltage to the plate line by connecting the positive voltage source to the ferroelectric capacitor.

19. The electronic memory apparatus of claim **12**, further comprising:

a plate line in electronic communication with the ferroelectric capacitor, wherein the controller is operable to:

apply a negative voltage to the plate line by connecting the negative voltage source to the ferroelectric capacitor.

20. The electronic memory apparatus of claim **12**, wherein a voltage of the negative voltage source is based at least in part on the threshold.

21. An electronic memory apparatus, comprising:

a ferroelectric memory cell that comprises a ferroelectric capacitor in electronic communication with a digit line;

means for connecting a positive voltage source to the ferroelectric capacitor; and

means for connecting a negative voltage source to the ferroelectric capacitor after a voltage of the digit line reaches a threshold.

22. The apparatus of claim 21, further comprising:

means for comparing the voltage of the digit line to a ground reference after a negative voltage is applied to the ferroelectric capacitor.

23. The apparatus of claim 22, further comprising:

means for determining a logic value of the ferroelectric memory cell based at least in part on a comparison of the voltage of the digit line to the ground reference.

24. The apparatus of claim 21, further comprising:

means for determining that a voltage of the digit line has reached the threshold in response to a positive voltage applied to the ferroelectric capacitor.

25. The apparatus of claim 24, further comprising:

means for determining that a voltage of the positive voltage source has been applied to the ferroelectric capacitor for a predetermined duration; and

means for determining that the voltage of the digit line has reached the threshold based at least in part on the means for determining that the voltage of the positive voltage source has been applied for the predetermined duration.

26. The apparatus of claim 24, further comprising:

means for determining that a rate of change of the voltage of the digit line has reached the threshold.

27. An electronic memory apparatus, comprising:

a ferroelectric memory cell that comprises a ferroelectric capacitor in electronic communication with a digit line and a first selection component;

a reference capacitor in electronic communication with the digit line via a

second selection component;

means for connecting a first voltage source to the ferroelectric capacitor; and

means for connecting a second voltage source to the reference capacitor, wherein an output of the second voltage source is an inverse of an output of the first voltage source.

28. The apparatus of claim 27, further comprising:

means for activating the first selection component to perform a read operation of the ferroelectric memory cell; and

means for activating the second selection component to transfer a charge of the reference capacitor to the digit line during the read operation.

29. The apparatus of claim 27, further comprising:

means for comparing a voltage of the digit line to a ground reference after a voltage of the second voltage source is applied to the reference capacitor.

30. The apparatus of claim 29, further comprising:

means for determining a logic value of the ferroelectric memory cell based at least in part on a comparison of the voltage of the digit line to the ground reference.

31. The apparatus of claim 27, further comprising:

means for virtually grounding the digit line before connecting the first voltage source to the ferroelectric capacitor or the second voltage source to the reference capacitor.