

WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:
lower electrodes, each lower electrode of the lower electrodes comprising an inner sidewall surrounding an inner space;
an upper support layer on top surfaces of the lower electrodes, the upper support layer being in the inner spaces surrounded by the inner sidewall of the lower electrodes; and
an upper electrode on the upper support layer, the upper electrode filling first and second regions, the second region penetrating the upper support layer, and the first region extending from the second region into between the lower electrodes,
wherein each of the lower electrodes includes:
a first portion overlapping with the first region, a top surface of the first portion being exposed by the upper support layer, and
a second portion covered by the upper support layer, the second portion having a vertical part and a horizontal part, the horizontal part electrically connecting bottoms of the first portion and the vertical part of the second portion, and a top surface of the vertical part of the second portion being in contact with the upper support layer.
2. The semiconductor memory device as claimed in claim 1, wherein the top surface of the first portion is at a lower level than the top surface of the vertical part of the second portion.
3. The semiconductor memory device as claimed in claim 1 or claim 2, wherein the upper support layer is on an upper portion of an outer sidewall of the second portion.

4. The semiconductor memory device as claimed in claim 3, wherein a bottom surface of the upper support layer in the inner space is at a lower level than a bottom surface of the upper support layer on the upper portion of the outer sidewall of the second portion.

5. The semiconductor memory device as claimed in claim 1 or claim 2, further comprising a lower support layer on outer sidewalls of the lower electrodes, the lower support layer being under the upper support layer.

6. The semiconductor memory device as claimed in claim 5, wherein the upper electrode penetrates a portion of the lower support layer on an outer sidewall of the first portion, and the upper electrode does not penetrate a portion of the lower support layer on an outer sidewall of the second portion.

7. The semiconductor memory device as claimed in any one of claims 1 to 6, wherein the upper support layer is in contact with the inner sidewalls of the lower electrodes and is spaced apart from bottom surfaces of the lower electrodes.

8. The semiconductor memory device as claimed in any one of claims 1 to 7, wherein the upper support layer includes at least one of SiOC, SiBN, SiCN, doped SiN, or Si.

9. The semiconductor memory device as claimed in any one of claims 1 to 5, wherein sidewalls of the second portion are in contact with the upper support layer.

10. The semiconductor memory device as claimed in claim 9, wherein a contact area between the upper support layer and an inner sidewall of the second portion is greater than a contact area between the upper support layer and an outer sidewall of the second portion.

11. The semiconductor memory device as claimed in any one of claims 1 to 10, wherein each of the lower electrodes has a U-shape when viewed in a cross-sectional view.

12. The semiconductor memory device as claimed in any one of claims 1 to 11, further comprising a dielectric layer between the upper electrode and the lower electrodes, and between the upper electrode and the upper support layer,

wherein the dielectric layer is in contact with the top surface of the first portion, and

wherein the dielectric layer is spaced apart from the top surface of the second portion.

13. The semiconductor memory device as claimed in any one of claims 1 to 3, wherein the inner space between a bottom surface of each of the lower electrodes and a bottom surface of the upper support layer in the inner space is filled with air.

14. The semiconductor memory device as claimed in any one of claims 1 to 13, wherein the second portion does not vertically overlap with the first region.

15. A semiconductor memory device, comprising:

lower electrodes, each lower electrode of the lower electrodes comprising an inner sidewall surrounding an inner space;

an upper support layer on top surfaces of the lower electrodes, the upper support layer being in the inner spaces surrounded by the inner sidewall of the lower electrodes; and

an upper electrode on the upper support layer, the upper electrode filling first and second regions, the second region penetrating the upper support layer, and the first region extending from the second region into between the lower electrodes,

wherein each of the lower electrodes includes:

a first portion overlapping with the first region, the first portion not overlapping with the upper support layer in a vertical direction, and

a second portion covered by the upper support layer, the second portion having a vertical part and a horizontal part, the horizontal part electrically connecting bottoms of the first portion and the vertical part of the second portion, and a top surface of the vertical part of the second portion vertically overlapping with the upper support layer.

16. The semiconductor memory device as claimed in claim 15, wherein a top surface of the first portion is at a lower level than the top surface of the vertical part of the second portion.

17. The semiconductor memory device as claimed in claim 15 or claim 16, wherein the upper support layer is on an upper portion of an outer sidewall of the second portion.

18. The semiconductor memory device as claimed in claim 17, wherein a bottom surface of the upper support layer in the inner space is at a lower level than a bottom surface of the upper support layer on the outer sidewall of the second portion.

19. The semiconductor memory device as claimed in any one of claims 15 to 18, wherein the upper support layer is in contact with the inner sidewalls of the lower electrodes and is spaced apart from bottom surfaces of the lower electrodes.

20. A semiconductor memory device, comprising:
lower electrodes, each lower electrode of the lower electrodes comprising an inner sidewall surrounding an inner space;
an upper support layer on top surfaces of the lower electrodes, the upper support layer being in the inner spaces surrounded by the inner sidewall of the lower electrodes; and

an upper electrode on the upper support layer, the upper electrode filling first and second regions, the second region penetrating the upper support layer, and the first region extending from the second region into between the lower electrodes,

wherein each of the lower electrodes includes:

a first portion overlapping with the first region, an outer sidewall of the first portion being spaced apart from the upper support layer, and

a second portion covered by the upper support layer, an outer sidewall of the second portion being in contact with the upper support layer,

wherein sidewalls of the second portion are in contact with the upper support layer, and

wherein a contact area between the upper support layer and an inner sidewall of the second portion is greater than a contact area between the upper support layer and the outer sidewall of the second portion.