

Description

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a fuzzy inference apparatus for conducting a fuzzy inference and to a function generating unit to be employed, for example, in a membership function circuit or a membership function generator of a fuzzy inference apparatus.

Description of the Prior Art

An fuzzy inference is achieved in accordance with rules in the form of If ... then ... (modus ponens). The rule is represented in a format "If x is A and Y is B and z is C, then w is D."

In this representation, x, y, and z are input variables of an antecedent, A, B, and C are membership functions thereof, w is a variable of a consequent, and D is a membership function thereof.

In the example above, the antecedent includes three kinds of input variables. In a case of two kinds thereof, the rule is expressed as follows.

"If x is A and y is B, then z is C." Namely, x and y are input variables of an antecedent, A and B are membership functions thereof, z is a variable of a consequent, and C is a membership function thereof in this representation.

The membership functions such as A to D are represented, for example, with linguistic information associated with PL, PM, PS, ZR, NS, NM, NL, etc. In these information items, P, N, L, M, and S denote positive, negative, large, medium, and small, respectively. In consequence, expressions PL and NS stand for positive large and negative small, respectively. ZR indicates almost zero. The linguistic information may be expressed, for example, with binary codes each comprising a plurality of bits.

FIG. 1 shows a conventional fuzzy inference apparatus, which includes a plurality (associated with a number of rules to be established) of individual inference sections or engines 100 and an integrator section 110 connected thereto. Each inference section 100 comprises membership function circuits (to be abbreviated as MFC herebelow) 101, 102, and 103 each being supplied with an input variable to produce a signal (e.g. a voltage signal) representing an associated value of a membership of an antecedent, a membership function generator (to be abbreviated as MFG herebelow) 105 for generating a signal representing a membership function of a consequent (e.g. a voltage signal distributed onto 25 lines, which transmit the voltage distribution and which are represented by a hatched bus in FIG.1; reference is to be made to the U.S. Patent Application Serial No.07/116,777 and the European Patent Application No. 87 116 529.6.), a logic intersection circuit 104 for con-

ducting an MIN operation on outputs from the MFCs 101 to 103, and a logic union circuit 106 for computing an MIN operation on outputs from the logic intersection circuit 104 and the MFG 105. Each of the MFCs 101 to 103 is supplied with a reference voltage (to be abbreviated as R.V. in drawings) corresponding to linguistic information (to be abbreviated as L.I. in drawings), so as to be set to produce a membership function conforming to a rule. Moreover, other parameters of the membership function outputted from the MFC is set by use of a parameter setting unit not shown. The reference voltage defines a peak position (center position) of the membership function. In this configuration, the MFG 105 is supplied with a code representing linguistic information to produce a membership function associated with the linguistic information. The concluder section 110 includes a logic union circuit 111 for achieving an MAX operation on the membership functions produced from the inference sections 100 and a defuzzifier 112 for defuzzifying an output from the logic union circuit 111 to produce a determinant output. The logic union circuit 111 produces a fuzzy output.

As described above, the conventional fuzzy inference apparatus is provided with an MFC and an MFG for each rule (i.e. for each individual inference section 100). Even a membership function represented with the same linguistic information is required to be set each time the function is assigned to a rule. In consequence, there arise problems that an error occurs in the setting operation and that the setting operation requires a long period of time.

Furthermore, when using such a conventional fuzzy inference apparatus, in a case where two or more inference systems are provided and the membership functions vary between the respective inference systems, it is necessary to prepare the fuzzy inference apparatuses as many as there are inference systems.

Referring now to FIG. 2, a description will be given of the fuzzy inference process in the individual inference section in a case of two input variables.

The MFCs 101 and 102 are respectively supplied with inputs x_0 and y_0 such that outputs a and b therefrom are fed to the logical intersection circuit 104. This circuit 104 selects the smaller of the inputs, namely, the output b in this case, so as to output the signal b therefrom. On the other hand, the MFG 105 produces the membership function C. The function C and the output b from the circuit 104 are subjected to an MIN operation in the logic union circuit 106.

As described above, since the MFG 105 outputs a voltage signal which is distributed on a plurality of signal lines to represent a predetermined membership function, the output signal from the MFG 105 is expressed as a set of voltage C_i ($i = 1$ to n) as shown in FIG. 3. In consequence, the results from the MIN operation are also represented as a set of voltage signals distributed on n signal lines and develop values in a discrete form.

Since the MFG 105 outputs a signal distribution on

a plurality of signal lines, such plural signal lines are required not only in each inference section 100 but also in the determinant or concluder section 110, which increases the size of the circuit and causes the circuit configuration to be complex. Since the membership function is expressed as a set of signals in a discrete form, there arises also a problem that the shape of the function is restricted by the number of signal lines.

Incidentally, in a fuzzy inference apparatus, a membership function circuit and a membership function generator circuit are necessary as described above. In a case where the membership function circuit or the membership function generator circuit is implemented in a digital circuit, there are in general employed a memory method in which a function value (an output value) is stored in a predetermined location to be accessed by use of a variable value (an input value) as an address thereof or a method in which a form or format of a function formula is registered such that an input value is assigned thereto so as to produce an output value.

However, in the memory method above, in order to improve the precision of the function value to be produced, the interval between variables as addresses is required to be minimized, which leads to a disadvantage that a large memory and a considerable manual operation are necessary for setting the membership function. Moreover, in a case of a membership function representing senses of a human, it is difficult to establish quite complicated items for the senses at the setting phase, and such items do not develop so significant functions.

In the latter case of the method above, since the membership function value is to be computed by a software program, there has been a problem that a long period of time is required.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention is to provide a function generating unit in which when a membership function is registered, the variable values to be plotted is minimized and a resolution is increased, thereby improving the inference precision. A fuzzy inference engine according to the invention is characterized by the features disclosed in claim 1.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects and advantages of the present invention will become apparent by reference to the following description and accompanying drawings wherein:

FIG. 1 is a schematic diagram showing the constitution of a conventional fuzzy inference apparatus or engine;

FIGS. 2 and 3 are schematic diagrams showing a fuzzy inference procedure;

FIG. 4 is a block diagram schematically showing the configuration of a fuzzy inference engine as a first embodiment according to the present invention;

FIG. 5 is a diagram showing the constitution of a membership function circuit array;

FIG. 6 is a schematic diagram showing the constitution of a membership function generator circuit array;

FIG. 7 is a circuit diagram schematically showing an example of the membership function circuit;

FIG. 8 and FIGS. 9a to 9d are diagrams showing control examples in which FIG. 8 is a diagram showing the configuration of a liquid surface level control and FIGS. 9a to 9d are graphs showing various membership functions;

FIG. 10 is an explanatory diagram useful to explain an operation in which membership function values are produced;

FIG. 11 is a block diagram schematically showing the configuration of a fuzzy inference engine as a second embodiment according to the present invention;

FIG. 12 is a diagram showing the constitution of a membership function circuit array set;

FIG. 13 is a schematic diagram showing the constitution of a membership function generator circuit array set;

FIG. 14 is a block diagram schematically showing the configuration of a fuzzy inference engine as a third embodiment according to the present invention;

FIG. 15 is a block diagram showing an embodiment according to the fourth and fifth inventions;

FIG. 16 is a graph showing input/output characteristics of a membership function circuit;

FIGS. 17a, 17b, and 17c are graphs showing waveforms of input/output signals in the respective blocks of an individual inference section;

FIGS. 18a, 18b, and 18c are graphs showing waveforms of input/output signals in the respective blocks of a concluder section;

FIGS. 19 to 22 are diagrams showing an embodiment according to the sixth invention in which:

FIG. 19 is a schematic diagram showing a fuzzy inference procedure associated with a rule;

FIG. 20 is a block diagram showing the constitution of a fuzzy inference engine as the embodiment;

FIG. 21 is a circuit diagram showing a specific example including a multiplier and an adder;

FIG. 22 is a circuit diagram showing another example of the multiplier;

FIG. 23 is a schematic block diagram showing the configuration of a fuzzy inference engine as a seventh embodiment according to the present invention;

FIG. 24 is a circuit diagram showing a concrete example of an amplifier disposed in the system of FIG. 23;

FIG. 25 is a circuit diagram showing a variation example of the inversion amplifier of FIG. 24;

FIG. 26 is a perspective view showing an appearance of a membership function circuit cartridge according to an eighth embodiment of the present invention;

FIG. 27 is a schematic block diagram showing a function generating arithmetic unit as a ninth embodiment according to the present invention; and

FIG. 28 is a graph for explaining the function of the function generating unit.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 4 shows the constitution of a fuzzy inference engine as an embodiment according to the first invention. Constituent components identical to those shown in FIG. 1 are assigned with the same reference numerals.

In association with three kinds of input variables, there are disposed three MFC arrays 11, 12, and 13. The MFC array 11 includes, as shown in FIG. 5, MFCs 101 of which the number is identical (seven in this example) to the number of kinds of linguistic information items. Each MFC is supplied with a reference voltage corresponding to one of linguistic information items PL to NL. FIG. 7 shows an example of a concrete constitution of the MFC 101. In this constitution, a reference voltage is applied to a terminal M such that a membership function is produced in a triangle form with the voltage as the center position (an input associated with the peak value of the membership function) of the triangle. In this case, the input and output voltages are represented as V_{IN} and V_{OUT} . The membership function of the triangle shape

has a gradient determined by resistors r_{E1} and r_{E2} . By changing these resistors r_{B1} and r_{B2} , the membership function may have a trapezoidal shape. In FIG. 5, the same input is supplied to seven MFCs 101, which then respectively produce function values with variables set as the inputs of the membership function representing preset linguistic information. Other MFC arrays 12 and 13 are also configured in the same fashion.

The configuration further includes individual inference sections 10. Each section 10 includes three selector circuits 21 to 23, which receive the outputs from the MFC arrays 11 to 13, respectively. Each of the selector circuits 21 to 23 is provided with a code representing linguistic information (abbreviated as L.I. in the figures as described above) such that of the outputs from the MFC arrays 11 to 13, membership function values associated with the linguistic information are respectively outputted from the selector circuits 21 to 23 so as to be fed to a logic intersection circuit 104.

The system includes an MFG array 15 constituted with seven MFGs 105 as shown in FIG. 6. Each MFG 105 generates a membership function associated with seven linguistic information items including PL to NL. The MFG array 105 delivers an output (a voltage distribution representing a membership function) to be supplied to a selector circuit 25. Among the seven kinds of membership functions thus supplied, the selector circuit 25 selects a function associated with the linguistic information inputted thereto so as to feed the selected function to a logic intersection circuit 106.

Since each MFG 105 is connected to 25 output lines, the MFG array 15 is linked to the selector circuit 25 by means of 25 x 7 output lines. However, if the MFC array 15 is designed to produce seven kinds of membership functions in a time-shared fashion and the selector 25 is configured to include a latch circuit so as to latch only the selected membership function, there need only 25 output lines. For a specific example of MFG, reference is to be made to the Japanese Patent Laid-Open Publication No. 63-129177 (associated with the U.S. Patent Application Serial Number 116,777 and E.P. Application Number 87 116 529.6 described above.)

As an example of control operation, let us consider a case where the liquid surface of a cistern is to be kept at a fixed level.

Assume here that inputs thereto are considered in association with a deviation e of the present liquid surface level with respect to a preset value (or level), a variation Δe of deviation, discharge flow rate Δu and that an output is represented by use of a valve opening OP to control the liquid flow rate. For these input and output data, the following linguistic information items are adopted.

Linguistic information for e
PL, PM, PS, ZR, NS, NM, and NL.

Linguistic information for Δe
P, ZR, and N.

Linguistic information for Δu
ZR, PS, PM, and PL.

Linguistic information for OP

PL, PM, PS, ZR, NS, NM, and NL.

FIGS. 9a to 9d show membership functions associated with these linguistic information items.

In the fuzzy inference engine or apparatus of FIG. 4, it is only necessary to dispose seven, three, and four MFCs 101 in the MFC array 11 for the deviation e , the MFC array 12 for the change Δe , and the MFC array 13 for the discharge flow rate Δu , respectively. The MFC array 15 for the valve opening OP includes seven MFCs 105 in this situation.

Measured inputs e_0 , Δe_0 , and Δu_0 are respectively supplied to the MFC arrays 11 to 13. The value e_0 is simultaneously supplied to the respective MFCs 101 of the MFC array 11 for the deviation e such that membership function values indicating a degree of adaptation to the respective linguistic information (a degree at which the value belongs to the membership function) are outputted in a parallel fashion. The membership function values are supplied in a parallel fashion to the inference sections 10 having rules employing the value e . By use of the selector circuit 21 of each inference section 10, either one of the input membership function values is selected depending on the supplied linguistic information. The similar processing is also achieved for Δe_0 and Δu_0 .

Also for the opening OP, membership functions associated with the respective linguistic information items are set to the MFC array 15 so as to be delivered to the respective inference section 10, so that based on the linguistic information of a rule associated with each inference section, the selection of membership function value is achieved for each inference section. A fuzzy inference is thus conducted to output a determinant value or an integrated of valve opening OP_0 from the defuzzifier 112.

FIG. 10 shows an operation in which when an input a is supplied to the MFC array 11, membership function values related to the respective linguistic information items are produced therefrom. For the input $a = -0.5$, the respective membership function values are obtained. In rule 1, the linguistic information is represented as $a = NS$, the selector circuit 21 selects a signal on a line of NS to develop an output 0.5. Similarly, in rule 2, a signal on a line of PM is selected to output a value 0.0.

In the embodiment above, although the fuzzy inference engine is of an analog type, it is natural that the present invention is applicable to an apparatus of a digital type.

FIG. 11 shows a configuration of a fuzzy inference engine as an embodiment according to the second invention. The same constituent elements as those of FIG. 1 are assigned with the same reference numeral. This embodiment is employed for a two inference systems.

In each individual inference section 90, there are disposed MFC sets each including two MFCs (namely, MFCs 101A and 101B, MFCs 102A and 102B, and MFCs 103A and 103B). This system further comprises variable selector circuits 91, 92, and 93 associated with the three

MFC sets, respectively. Each of the MFCs above is supplied with a reference voltage conforming to a preset rule. A concrete constitution of the MFCs are the same as that shown in FIG. 7.

FIG. 12 shows a configuration example of a set of MFCs 101A and 101B. Each MFC includes a selector as a variable selecting circuit 91. It is possible to register a variable name to the selector. When a variable name registered to the selector matches with a variable selection signal supplied thereto, the associated MFC is set to an active state to operate as a membership function circuit. It may also be possible that the MFCs 101A and 101B are caused to continuously operate as membership function circuits so as to selectively output signals therefrom depending on a variable selection signal. The similar operation is carried out in the other MFC sets respectively including the MFCs 102A and 102B and the MFCs 103A and 103B. The selected MFC output is supplied to the logic intersection circuit 104.

In a similar fashion, each inference section 90 includes the MFCs 105A and 105B and a variable selection circuit 95 for achieving a selection depending on a variable selection signal. FIG. 13 shows a configuration example of these constituent elements. Each of MFCs 105A and 105B includes a selector to which a variable name can be registered such that by one of the selectors having a variable name identical to a variable name supplied in a form of a variable selection signal sets the associated MFC 105A or 105B to an active state. Or, an output from the associated MFC is selectively obtained to be fed to the logic intersection circuit 106. For a specific example of the MFC, reference is to be made to, for example, the Japanese Patent Laid-Open No. 63-123177 as described above.

In the circuit constitution above, two systems of inference operations can be achieved in an online and time-series fashion by use of the same inference engine.

For example, assume here that two systems of inference operations are given as follows.

$$\text{if } a = A, b = B, c = C, \text{ then } u = U \quad (1)$$

$$\text{if } d = D, e = E, f = F, \text{ then } v = V \quad (2)$$

For the inference of expression (1), the variable selection signal line is supplied with a signal to select a membership function of expression (1). For the inference of expression (2), the variable selection signal line is supplied with a signal to select a membership function of expression (2). The operations are sequentially changed over therebetween so as to attain an output of the inference result, thereby enabling the two-system inference operation to be achieved by use of an inference engine or apparatus. In a configuration in which an output from one of two inference systems is kept retained so as to be employed as an input to other one inference system, a hierarchic inference can be accomplished in an inference engine.

FIG. 14 shows an embodiment of the inference engine in accordance with the third embodiment. In this constitution, with respect to inference sections 10, MFCs

and MFGs are externally disposed in association with all linguistic information items. The system comprises MFC array sets of MFC arrays 11A and 11B, MFC arrays 12A and 12B, and MFC arrays 13A and 13B and variable selector circuits 31, 32, and 33 for selecting either one of the associated MFC arrays depending on a variable selection signal. The variable selector circuits can be implemented by use of selectors described above. Each MFC array includes MFCs 101 of which the number is identical to that of kinds of linguistic information items (seven in this embodiment) as shown in FIG. 5.

All MFCs 101 constituting two MFC arrays of each MFC array set are supplied with the same input such that one of the MFCs 101 of the MFC arrays selected depending on the variable selection signal produces a function value corresponding to an input related to a membership function representing preset linguistic information. This is also the case for the other MFC array sets.

Each inference section 10 includes three selector circuits 21, 22, and 23, which are respectively supplied with outputs from the selected ones of the MFC arrays 11A and 11B, MFC arrays 12A and 12B, and MFC arrays 13A and 13B, respectively. The selector circuits 21, 22, and 23 are respectively supplied with codes representing linguistic information. Among the outputs from the MFC arrays above, the function values of the membership functions associated with these linguistic information items are delivered from the selector circuits 21, 22, and 23, respectively. The selector circuits 21, 22, and 23 deliver outputs therefrom to a logic intersection circuit 104.

Similarly, the system includes MFG array sets of MFG arrays 15A and 15B. Each MFG array is constituted with seven MFGs as shown in FIG. 6. Either one of each MFG array set is selected in a similar fashion depending on a variable selection signal. The selected MFG array 15A or 15B delivers an output (a voltage distribution representing a membership function) to a selector circuit 25. From seven kinds of membership functions, the selector circuit 25 selects a membership function corresponding to linguistic information supplied thereto so as to deliver the function to a logic intersection circuit 106.

Each MFG 105 is linked with 25 output lines; in consequence, the selected MFG array 15A or 15B is connected to the selector circuit 25 by means of 25 x 7 output lines. However, the MFG array 15A or 15B may be configured to produce seven kinds of membership functions in a time-shared manner and the selector circuit 25 includes a latch circuit such that only the selected membership function is latched therein, which necessitates only 25 output lines to be provided for the MFG arrays 15A and 15B.

Although the embodiment above includes a fuzzy inference engine of an analog type, it goes without saying that the present invention is also applicable to apparatuses of a digital type.

FIG. 15 shows a configuration of a fuzzy inference engine as an embodiment in accordance with the fourth and fifth inventions. The same constituent components

as those of FIG. 1 are assigned with the same reference numerals.

This system includes individual inference sections 40 each comprising an MFC 41 to produce a membership function of a consequent. The MFC 41 is supplied with a scan signal delivered from a scan waveform generator circuit 49. The scan signal has a fixed period and may be a sawtooth wave, a triangular wave, or the like. The MFC 41 supplies an output signal to a logic intersection circuit 42, which conducts an MIN operation between the received output signal and an output signal from a logic intersection circuit 104 so as to produce the MIN result as an output from the inference section 40.

The MFCs 101 to 103 and the MFC 41 can be configured with completely the same circuits. A concrete example of the configuration is as shown in FIG. 7. Each of the MFCs 101-103 is supplied with an input V_{IN} as an input signal thereto so as to deliver an output V_{OUT} to the logic intersection circuit 104. The MFC 41 receives as an input V_{IN} thereto an output scan signal from the scan waveform generator circuit 49. The output V_{OUT} is supplied to the logic intersection circuit 42.

FIG. 16 shows an example of relationships between the input V_{IN} and the output V_{OUT} of the MFC 41 in which the reference voltage applied to a terminal M is set to 2 V. The input V_{IN} is assumed to vary in a range from -5 V to +5 V.

FIGS. 17a, 17b, and 17c show along an axis of time (t) the input (scan) signal V_{IN} , the output signal V_{OUT} of the MFC 41, and the output signal from the logic intersection circuit 42 (the inference section 40) in a case where the MFC 41 is employed. The logic intersection circuit 104 producing a waveform of FIG. 17c delivers an output set to 3 V.

Since all inference sections 40 are supplied with the same scan signal, these sections output synchronized signals representing the respective inference results, which are fed to a concluder section 45.

The concluder section 45 includes a logic union circuit 46 for achieving an MAX operation on output signals from the inference sections 40, a discretizer circuit 47 for translating an output signal from the logic union circuit 46 into a set of signals distributed onto a plurality of lines, and a defuzzifier 48 for translating an output signal from the logic union circuit 46 into a signal representing a determinant value. These circuits 47 and 48 are also supplied with the output scan signal from the scan waveform generator circuit 49 so that the various kinds of arithmetic operations are accomplished at a timing synchronized with the scan signal.

The defuzzifier 48 comprises an integration circuit or a peak detector circuit so as to achieve the following operation as a defuzzification to attain a center of gravity CG(V).

$$CG(V) = \int u(t) \cdot V_m(t) dt / \int V_m(t) dt \quad (3)$$

where, $u(t)$ represents a scan signal and $V_m(t)$ stands for an output signal from the logic union circuit 46. The integration period is set to the period of the scan signal.

FIGS. 18a, 18b, and 18c show waveforms of the scan signal $u(t)$, the output $V_m(t)$ from the logic union circuit 46 and the dividend of expression (3). In this case, the logic union circuit 46 receives as one of the inputs a signal of FIG. 17c and as other one input a signal obtained when the output from the logic intersection circuit 104 is 1 V.

Next, a description will be given of an embodiment in accordance with the sixth invention.

FIG. 19 shows an inference procedure of a rule in a case of three kinds of input variables.

Assume here that for given inputs x_0, y_0, z_0 , etc., the result h is obtained through the MIN operation conducted on function values a, b , and c associated with the membership functions A, B , and C . Applying the MIN results to a membership function D of the consequent, a membership function S having a trapezoidal shape is obtained as indicated by a shade portion in FIG. 19. Namely, this is attained as an inference result from an individual inference section 100 (refer to FIG. 1 for details.)

In a concluder section 110, the inference results S are subjected to an MAX operation. In a case to attain a nonfuzzy output through a method of center of gravity, this section 110 computes the center of gravity from the result of the MAX operation.

If the membership function D of the consequent is horizontally symmetric with respect to the center d , the center of gravity CG is attained from the following expression.

$$CG = \sum_1 d_i \cdot h_i / \sum_1 h_i \quad \dots (4)$$

where, $i = 1$ to n and n is the number of rules and d_i indicates a position of center of the membership function D_i of the consequent.

FIG. 20 shows an example of a fuzzy inference engine capable of developing as the final output the center of gravity CG represented by expression (4). In this configuration, the same constituent components as those described above are assigned with the same reference numerals.

This system includes setting devices 51. To each setting device 51, a value is set to represent a center position d_i of the membership function D_i of the consequent. An MIN result h_i produced from a logic intersection circuit 104 is computed with the center position d_i by means of a multiplier 53 to attain a product $d_i \cdot h_i$. The MIN result h_i and the product $d_i \cdot h_i$ are outputted from an individual inference section 50.

The MIN result h_i is added to each other

$$\left(\sum_1 h_i \right)$$

in an adder 54 for all rules. Moreover, for all preset rules, the product $d_i \cdot h_i$ are similarly added

$$\left(\sum_1 d_i h_i \right)$$

by an adder 55. The results of additions carried out by these adders 54 and 55 are fed to a divider 56 to achieve the operation represented by the expression (4). In consequence, the divider 56 produces a final nonfuzzy output (center of gravity CG).

Comparing the circuit constitution of FIG. 20 with the conventional example of FIG. 1, the logic intersection circuits 106 and the MFGs are unnecessary in the embodiment of FIG. 20; furthermore, there need only two output terminals and two wiring lines. In addition, the concluder section 110 can be constituted with an adder and a divider, which simplifies the overall structure of the fuzzy inference engine.

FIG. 21 is a circuit diagram showing a specific example of the multiplier 53 and the adders 54 and 55 implemented by use of analog circuits.

The configuration includes an individual inference section in which a logic intersection circuit 104 produces an output value of a voltage h_i . The voltage h_i is applied to a resistor R , which flows a current h_i/R . The output voltage h_i is also supplied to a resistor r/d_i to flow a current $(h_i \cdot d_i)/r$. The resistance value of the resistor r/d_i is inversely proportional to a value d_i representing the center position of a membership function set to the consequent. That is, the resistor r/d_i constitutes the setting device 51 and the multiplier 53.

The configuration also includes a wired OR section 54A to conduct an addition of h_i/R . The resistor R and the wired OR 54A constitute the adder 54. The adder 55 comprises a wired OR 55A to achieve an addition of the current $(h_i \cdot d_i)/r$. An output from the wired OR 55A is supplied to a divider 56, which divides the output by an output from the wired OR 54A so as to output the result of the division as a nonfuzzy output.

FIG. 22 shows an example of variation of the resistor r/d_i in which the membership function of the consequent can be varied depending on given linguistic information. This configuration includes a parallel connection of resistors $r_{PL}, r_{PM}, r_{PS}, r_{ZR}, r_{NS}, r_{NM}$, and r_{NL} such that depending on the given linguistic information, one of the resistors is selected by an analog multiplexer 57. These resistors r_{PL} to r_{NL} have resistance values inversely proportional to values representing center positions of the membership functions PL to NL, respectively.

In the embodiment having the constitution above, as compared with the conventional structure of FIG. 1, the equivalent function can be developed by the fuzzy inference engine with a size thereof reduced to one third of the conventional system. Namely, the size of the body of the fuzzy inference engine and the cost thereof can be minimized.

The embodiment above includes the fuzzy inference engine constituted in a hardware system; however, the engine may be constructed with a software system employing the similar processing method (associated with the expression (4)). Also in such a software constitution, the number of processing operations can be reduced and hence the processing speed is accordingly in-

creased.

Incidentally, in the fuzzy inference engine of the embodiment above, all membership functions set to the consequents of rules are limited to the same form in which the width and the gradient are mutually identical among the functions. In short, it is impossible to set membership functions having different forms for the respective rules.

In consequence, although the system above can satisfactorily cope with a simple control, when it is necessary to alter the degree of importance for each rule or to vary the form of membership functions, the system cannot be efficiently applied to such a case.

An embodiment which solves the problems above according to the seventh invention will be described in detail with reference to FIGS. 23 to 25.

The configuration of FIG. 23 differs from that of FIG. 20 in that an amplifier (a coefficient device) 52 is connected between the logic intersection circuit 104 and the adder 54 as well as the multiplier 53. The logic intersection circuit 104 delivers an output h_i' to the amplifier 52, which amplifies the output h_i' with a preset gain (coefficient) K such that a result of the amplification is outputted as an output value h_i from the individual inference section 50. The output h_i is fed to the adder 54 and the multiplier 53.

FIG. 24 shows a concrete example of the constitution of the amplifier 52, which includes two inversion amplifiers 52A and 52B configured in a cascade connection. The amplifier 52A comprises an operational amplifier, an input resistor r_o thereof, and a feedback resistor K_r . Receiving an input h' , the amplifier 52A amplifies the input with an amplification factor $-K_r/r_o$. The amplifier 52B at the subsequent stage amplifies an input thereto by an amplification factor -1 . As a result, the input h' is multiplied by $K = K_r/r_o$, namely, the amplifier 52B produces an output signal $h = K \cdot h'$.

FIG. 25 shows an example of variation of the inversion amplifier 52A at the preceding stage. The feedback resistor circuit of the operational amplifier includes m resistors $K_{1r}, K_{2r}, \dots, K_{mr}$ connected in parallel and an analog multiplexer 58 for selecting either one of these resistors in response to a gain decision signal supplied thereto. When a gain decision signal is inputted to the analog multiplexer 58, one of the registers is selected depending on an indication content of the signal so as to vary the amplification factor K of the amplifier 52.

As described above, it is possible to multiply the output from the logic intersection circuit 104 by a coefficient. In consequence, depending on the degree of importance of a rule or the like, the fuzzy inference engine can be arbitrarily adjusted, thereby improving the degree of freedom of adjustment.

It goes without saying that the seventh invention can also be materialized by use of a software system.

In accordance with the eighth invention, the MFCs 101 to 103 of the antecedent and the MFGs 105 of the consequent are respectively housed in detachable car-

tridges, which are to be installed in the body of the fuzzy inference engine.

FIG. 26 shows an external appearance of an MFC cartridge 60, which comprises eight plugs 60b serving as terminals respectively associated with input/output signals and power supply voltage. The body of the fuzzy inference engine includes sockets corresponding to the plugs 60b. On the upper surface of the cartridge 60, there are disposed four trimmers 60a related to variable registers r_{E1}, r_{B1}, r_{E2} , and r_{B2} (refer to FIG. 7 for details). By turning these trimmers by means of a screwdriver, the associated resistance values can be altered to change the shape and position of membership functions. When the adjustment is beforehand achieved by use of the trimmers 60a, the membership functions can be set only by installing the cartridges 60 into the sockets. The MFC cartridges are also configured in the same fashion.

If the MFC arrays 11 to 13 and the MFG array 15 of FIG. 4, the MFC arrays 11A to 13B and MFG arrays 15A and 15B of FIG. 14, and all MFCs and MFGs included in these arrays are designed to be detachably installed in the fuzzy inference engine by means of the plugs and sockets, the replacement of arrays as well as switching thereof are facilitated.

In addition, the MFCs 101A to 103B and MFGs 105A and 105B of FIG. 11 need only be housed in the respective cartridges to be detachably inserted into sockets.

FIG. 27 is a block diagram showing a function generating unit as an embodiment according to the ninth embodiment, whereas FIG. 28 is a graph useful to explain a function generated by the function generating unit of FIG. 27. Variable values are supplied in a form of 8-bit data (x) to this unit. The 8-bit data (x) is subdivided by a bit distributor 71 into four high-order bits (x_0) and four low-order bits (x). The value of four high-order bits (x_0) is supplied as an address signal to a memory 73a and to an adder 72, which adds one to the received value. The adder 72 delivers the resultant value to a memory 73b. In the memories 73a and 73b, the same data are respectively stored at the same associated addresses with a fixed plotting interval (dots shown in FIG. 28 indicate plotted positions and are stored in the memory.) From the memory 73a, the system reads out an output (y_0) by use of an address x_0 so as to supply the output (x_0) to adders 74 and 76. In the adder 74, the value is processed as a negative value ($-y_0$), namely, a subtraction is actually conducted. The adder 74 is also provided with an output (y_1) from the memory 73b. In consequence, the adder 74 produces a difference ($y_1 - y_0$) between the outputs from the memories 73b and 73a, respectively. The resultant value is fed to a multiplier 75, which multiplies the value ($y_1 - y_0$) by the value of the four inputted low-order bits ($x/16$) to output the result to the adder 76. In the adder 76, the multiplication result is added to the output y_0 from the memory 73a to produce the result as a function value y .

Incidentally, in the memories 73a and 73b, if the same data items are stored at addresses having differ-

ence of one address unit therebetween (i.e. at an address where data x_0 is stored in the memory 73a, data x_1 is stored in the memory 73b), the adder 72 is unnecessary. Furthermore, in a case where the operation speed is not critical, it is possible to employ only one memory so as to sequentially read out x_0 and x_1 therefrom.

In this embodiment, the description has been given of a membership function circuit of a fuzzy inference engine. However, the invention described above is also applicable to apparatuses such as a standard pattern storage of a pattern identifier.

While the particular embodiment of the invention has been shown and described, it will be obvious to those skilled in the art that various changes and modifications may be made without departing from the fuzzy inference machine as claimed in claims 1 and 2.

Claims

1. A fuzzy inference engine for performing fuzzy reasoning processing in accordance with preset rules, each said rule being expressed as a combination of antecedent and consequent, having:

antecedent processing means (101, 102, 103, 104) for executing antecedent operation, in which input signals are applied to antecedent membership functions, to output an antecedent processing result (h_i) for said each rule;
consequent processing means (51, 53) for executing consequent operation, in which the antecedent processing results are applied to consequent functions, to output a consequent processing result for each said rule; and
defuzzifying means (54, 55, 56) for calculating a center of gravity (CG) of the consequent results;

characterized in that:

said consequent processing means includes setting means (51) provided for each said rule for setting a representative position (d_i) of the consequent function (D_i) of each said rule, and first arithmetic means (53) for multiplying, for each said rule, the antecedent processing result (h_i) outputted from said antecedent processing means (101, 102, 103, 104) and a value (d_i) representing the representative position set by said setting means (51);

said defuzzifying means includes second arithmetic means (55) for performing an addition ($\sum d_i \cdot h_i$) of the component ($d_i \cdot h_i, \dots, d_n \cdot h_n$) representing the products obtained from said first arithmetic means (53),
third arithmetic means (54) for performing an addition ($\sum h_i$) of the component ($h_i, \dots, h_n$) outputted from said antecedent processing means

(101, 102, 103, 104), and
fourth arithmetic means (56) for dividing the result ($\sum d_i \cdot h_i$) of the addition performed by said second arithmetic means (55), by the result ($\sum h_i$) of the addition performed by said third arithmetic means (54).

2. A fuzzy inference engine according to claim 1 further including coefficient means (52) for multiplying an output from said antecedent processing means (101, 102, 103, 104) by a coefficient K_i specified for each said rule.

Patentansprüche

1. Fuzzy-Schlußfolgerungswerk zur Durchführung von Fuzzy-Schlußfolgerungsverarbeitung gemäß vor-
eingestellter Regeln, wobei jede dieser Regeln als eine Kombination aus Bedingung und Folge ausgedrückt wird, mit

Bedingungs-Verarbeitungsmitteln (101, 102, 103, 104) zum Ausführen einer Bedingungs-Operation, in welcher Eingangssignale auf Bedingungs-Zugehörigkeitsfunktionen angewandt werden, zur Ausgabe eines Bedingungs-Verarbeitungsergebnisses (h_i) für jede der Regeln,

Folge-Verarbeitungsmitteln (51, 53) zum Ausführen einer Folge-Operation, in welcher die Bedingungs-Verarbeitungsergebnisse auf Folge-Funktionen angewandt werden, zur Ausgabe eines Folge-Verarbeitungsergebnisses für jede der Regeln, und

Defuzzifizierungsmitteln (54, 55, 56) zum Berechnen eines Schwerpunkts (CG) der Folge-Ergebnisse,

dadurch gekennzeichnet, daß

die Folge-Verarbeitungsmittel Einstellmittel (51), die für jede der Regeln vorgesehen sind, zur Einstellung einer repräsentativen Lage (d_i) der Folge-Funktion (D_i) jeder der Regeln, und

erste Rechenmittel (53) zum Multiplizieren, für jede der Regeln, des Bedingungs-Verarbeitungsergebnisses (h_i), das von den Bedingungs-Verarbeitungsmitteln (101, 102, 103, 104) ausgegeben wird, mit einem Wert (d_i), der die mit den Einstellmitteln (51) eingestellte repräsentative Lage darstellt, enthalten,

die Defuzzifizierungsmittel zweite Rechenmittel (55) zur Durchführung einer Addition ($\sum d_i \cdot h_i$) der die mit den ersten Rechenmitteln (53) erhaltenen Produkte darstellenden Komponente ($d_i \cdot h_i, \dots, d_n \cdot h_n$), dritte Rechenmittel (54) zur Durchführung einer Addition ($\sum h_i$) der von den Bedingungs-Verar-



ence of one address unit therebetween (i.e. at an address where data x_0 is stored in the memory 73a, data x_1 is stored in the memory 73b), the adder 72 is unnecessary. Furthermore, in a case where the operation speed is not critical, it is possible to employ only one memory so as to sequentially read out x_0 and x_1 therefrom.

In this embodiment, the description has been given of a membership function circuit of a fuzzy inference engine. However, the invention described above is also applicable to apparatuses such as a standard pattern storage of a pattern identifier.

While the particular embodiment of the invention has been shown and described, it will be obvious to those skilled in the art that various changes and modifications may be made without departing from the fuzzy inference machine as claimed in claims 1 and 2.

Claims

1. A fuzzy inference engine for performing fuzzy reasoning processing in accordance with preset rules, each said rule being expressed as a combination of antecedent and consequent, having:

antecedent processing means (101, 102, 103, 104) for executing antecedent operation, in which input signals are applied to antecedent membership functions, to output an antecedent processing result (h_i) for said each rule;
consequent processing means (51, 53) for executing consequent operation, in which the antecedent processing results are applied to consequent functions, to output a consequent processing result for each said rule; and
defuzzifying means (54, 55, 56) for calculating a center of gravity (CG) of the consequent results;

characterized in that:

said consequent processing means includes setting means (51) provided for each said rule for setting a representative position (d_i) of the consequent function (D_i) of each said rule, and first arithmetic means (53) for multiplying, for each said rule, the antecedent processing result (h_i) outputted from said antecedent processing means (101, 102, 103, 104) and a value (d_i) representing the representative position set by said setting means (51);

said defuzzifying means includes second arithmetic means (55) for performing an addition ($\sum d_i \cdot h_i$) of the component ($d_i \cdot h_i, \dots, d_n \cdot h_n$) representing the products obtained from said first arithmetic means (53), third arithmetic means (54) for performing an addition ($\sum h_i$) of the component ($h_i, \dots, h_n$) outputted from said antecedent processing means

(101, 102, 103, 104), and

fourth arithmetic means (56) for dividing the result ($\sum d_i \cdot h_i$) of the addition performed by said second arithmetic means (55), by the result ($\sum h_i$) of the addition performed by said third arithmetic means (54).

2. A fuzzy inference engine according to claim 1 further including coefficient means (52) for multiplying an output from said antecedent processing means (101, 102, 103, 104) by a coefficient K_i specified for each said rule.

Patentansprüche

1. Fuzzy-Schlußfolgerungswerk zur Durchführung von Fuzzy-Schlußfolgerungsverarbeitung gemäß vor-
eingestellter Regeln, wobei jede dieser Regeln als eine Kombination aus Bedingung und Folge ausgedrückt wird, mit

Bedingungs-Verarbeitungsmitteln (101, 102, 103, 104) zum Ausführen einer Bedingungs-Operation, in welcher Eingangssignale auf Bedingungs-Zugehörigkeitsfunktionen angewandt werden, zur Ausgabe eines Bedingungs-Verarbeitungsergebnisses (h_i) für jede der Regeln,

Folge-Verarbeitungsmitteln (51, 53) zum Ausführen einer Folge-Operation, in welcher die Bedingungs-Verarbeitungsergebnisse auf Folge-Funktionen angewandt werden, zur Ausgabe eines Folge-Verarbeitungsergebnisses für jede der Regeln, und

Defuzzifizierungsmitteln (54, 55, 56) zum Berechnen eines Schwerpunkts (CG) der Folge-Ergebnisse,

dadurch gekennzeichnet, daß

die Folge-Verarbeitungsmittel

Einstellmittel (51), die für jede der Regeln vorgesehen sind, zur Einstellung einer repräsentativen Lage (d_i) der Folge-Funktion (D_i) jeder der Regeln, und

erste Rechenmittel (53) zum Multiplizieren, für jede der Regeln, des Bedingungs-Verarbeitungsergebnisses (h_i), das von den Bedingungs-Verarbeitungsmitteln (101, 102, 103, 104) ausgegeben wird, mit einem Wert (d_i), der die mit den Einstellmitteln (51) eingestellte repräsentative Lage darstellt, enthalten, die Defuzzifizierungsmittel

zweite Rechenmittel (55) zur Durchführung einer Addition ($\sum d_i \cdot h_i$) der die mit den ersten Rechenmitteln (53) erhaltenen Produkte darstellenden Komponente ($d_i \cdot h_i, \dots, d_n \cdot h_n$),

dritte Rechenmittel (54) zur Durchführung einer Addition ($\sum h_i$) der von den Bedingungs-Ver-



beutungsmitteln (101, 102, 103, 104) ausgegebenen Komponente ($h_1, \dots, h_n$), und vierte Rechenmittel (56) zum Dividieren des Ergebnisses ($\sum d_i h_i$) der mit den zweiten Rechenmitteln (55) durchgeführten Addition durch das Ergebnis ($\sum h_i$) der mit den dritten Rechenmitteln (54) durchgeführten Addition enthalten.

2. Fuzzy-Schlußfolgerungswerk nach Anspruch 1, welches ferner Koeffizientenmittel (52) zum Multiplizieren einer Ausgabe der Bedingungs-Verarbeitungsmittel (101, 102, 103, 104) mit einem Koeffizienten K_i , der für jede der Regeln spezifiziert ist, enthält.

Revendications

1. Moteur d'inférence floue pour effectuer un traitement de raisonnement flou en fonction de règles fixées à l'avance, chaque dite règle étant exprimée par une association d'un antécédent et d'une conséquence, comportant:

des moyens de traitement d'antécédents (101, 102, 103, 104) pour exécuter une opération d'antécédents, dans lesquels des signaux d'entrée sont appliqués à des fonctions de membres d'antécédents, pour délivrer en sortie un résultat de traitement d'antécédents (h_i) pour chaque dite règle;

des moyens de traitement de conséquences (51, 53) pour exécuter une opération de conséquences, dans lesquels les résultats des traitements d'antécédents sont appliqués à des fonctions de conséquences, pour délivrer en sortie un résultat de traitement de conséquences pour chaque dite règle; et

des moyens pour rendre non flou (54, 55, 56) pour calculer un centre de gravité (CG) des résultats de conséquences;

caractérisé en ce que:

lesdits moyens de traitement de conséquences comportent

des moyens de détermination (51) prévus pour chaque règle fixée à l'avance, pour fixer une position centrale (d_i) de la fonction de conséquence (D_i) de chaque dite règle; et

des premiers moyens arithmétiques (53), pour multiplier, pour chaque dite règle, le résultat du traitement d'antécédent (h_i) délivré en sortie par lesdits moyens de traitement d'antécédents (101, 102, 103, 104), et une valeur (d_i) représentant la position représentative fixée par lesdits moyens de détermination (51);

lesdits moyens pour rendre non flou comportent un deuxième moyen arithmétique (55), pour

effectuer une addition ($\sum d_i h_i$) de la composante ($d_i h_i, \dots, d_n h_n$) représentant les produits obtenus par lesdits premiers moyens arithmétiques (53);

un troisième moyen arithmétique (54), pour effectuer une addition ($\sum h_i$) de composante ($h_1, \dots, h_n$), délivrée en sortie par lesdits moyens de traitement d'antécédents (101, 102, 103, 104), et

un quatrième moyen arithmétique (56), pour diviser le résultat ($\sum d_i h_i$) de l'addition effectuée par ledit deuxième moyen arithmétique (55), par le résultat ($\sum h_i$) de l'addition effectuée par ledit troisième moyen arithmétique (54).

2. Moteur d'inférence floue selon la revendication 1, comportant en outre des moyens de coefficients (52), pour multiplier une sortie provenant desdits moyens de traitement d'antécédents (101, 102, 103, 104) par un coefficient K_i spécifié pour chaque dite règle.