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Background of the invention

The present invention relates to a timing recovery circuit and, more particularly, to a circuit for recovering timing signals out of split-phase or Manchester coded data.

There are both analog and digital versions of such a timing recovery circuit. An example of analog type timing recovery circuit is described in The Bell System Technical Journal, Vol. 58, No. 1, January 1979, pp. 139—143. An analog type timing recovery circuit extracts the timing component of a frequency equal to half the bit rate of a preamble or dotting section of "1" and "0" added before the data, and achieves synchronization by using the extracted timing component. This kind of analog type recovery circuit has the disadvantage of complex circuitry, which prevents ready large-scale integration.

A digital type timing recovery circuit, as will be described afterwards with reference to some of the accompanying drawings, readily permits large-scale integration. However, it has its own problem that, if either "1" or "0" emerges consecutively in the data, the varying points of the data, which should be at the trailing edge of the clock, will be displaced by 180 degrees, making synchronization impossible. To avoid the phase displacement of the regenerated clock, the conventional digital timing recovery circuit controls an oscillator for timing synchronization only during the dotting section and the synchronized oscillator is maintained during the date section. In the case, however, the stability of the oscillator may pose a problem. With an insufficiently stable oscillator, the frame length of the data cannot be made great enough, resulting in a poor efficiency of channel utilization. On the other hand, a sufficiently stable oscillator would be too expensive and constitute a disadvantage.

Summary of the invention

An object of the present invention, therefore, is to provide a digital type timing recovery circuit for split-phase or Manchester coded data, which permits ready large-scale integration.

Another object of the invention is to provide a digital type timing recovery circuit for Manchester coded data, which permits the frame length of data to be made substantially great without having to use a highly stable oscillator.

Still another object of the invention is to provide a digital type timing recovery circuit for Manchester coded data, which can supply stable timing signals even if either "1" or "0" consecutively is contained in the data.

According to the present invention, there is provided a timing recovery circuit comprising: means for detecting the varying points of a split-phase signal having a pattern of the repetition of logical "1" and "0" at its beginning; voltage-controlled oscillator (VCO) means for generating a signal whose frequency is twice as high as that of the timing signal of the split-phase signal and controlling the frequency of the generated signal in response to a control signal; means for dividing by two the output frequency of the VCO means; selector means for selectively supplying the output of the VCO means and that of the frequency dividing means; phase detector means for phase-comparing the output of the varying point detector means and that of the selector means, and supplying the VCO means with a signal indicating the relative delay or advance between the two outputs as the control signal; and control means for controlling the selector means so that it selects the output of the frequency dividing means during the repetitive pattern of logical "1" and "0" and that of the VCO means elsewhere.

Brief description of the drawings

The foregoing and other objects, features and advantages of the present invention will become more apparent from the detailed description hereunder taken in conjunction with the accompanying drawings, wherein:

Figure 1 is a block diagram showing a conventional digital type timing recovery circuit for Manchester coded data;

Figures 2A to 2D are diagrams showing waveforms in different parts of the timing recovery circuit shown in Figure 1;

Figure 3 is a block diagram showing a digital type timing recovery circuit for Manchester coded data, which is a preferred embodiment of the invention;

Figures 4A to 4D are diagrams showing waveforms in different parts of the timing recovery circuit shown in Figure 3;

Figure 5 is a detailed diagram of a phase detector of the circuit illustrated in Figure 3;

Figures 6A to 6G are diagrams showing waveforms in different parts of the phase detector shown in Figure 5; and

Figure 7 is a detailed diagram of a frame synchronization signal detector of the circuit shown in Figure 3.

Detailed description of the invention

To facilitate understanding of the present invention, a timing recovery circuit of the prior art will be described first. Referring to Figure 1, the varying points of an input split-phase or Manchester coded signal A are detected by a differentiator circuit 1, and supplied to a phase detector 2, which phase-compares the varying points of the input signal A and a regenerated clock f_2 from a digital voltage-controlled oscillator (VCO) 3 and controls the oscillating frequency of the VCO 3 with the resultant phase difference signal. Control is thereby so effected that the trailing edge of the output clock f_2 of the VCO 3 concur with the varying points of the input signal A.

Figure 2A shows the split-phase signal A, in which are provided data (DATA) and, before them, a dotting section (DOT), which consists of repetitions of logical "1" and "0", plus a frame synchronization (sync) signal (FS) between DATA

and DOT if it is a synchronized type communication system. Figure 2B shows the extracted clock f_2, so controlled that the varying points of the signal A concur with the trailing edges of the clock f_2. However, if either "1" or "0" emerges consecutively in a signal later than the frame sync signal FS, a varying point may also occur at any other point displaced by 180 degrees than the trailing edge of the clock f_2, thereby preventing proper synchronization. For this reason, the frame sync signal FS is detected by a split-phase signal-to-non-return to zero (SPL-NRZ) converter 4 and a frame sync signal detector circuit 5, and the detected signal (D) is used to render the differentiator 1 non-operative. Jitters occurring in the regenerated clock are thereby removed.

However, since the phase of the clock is not adjusted during the DATA section in the timing recovery circuit of Figure 1 as stated above, there is needed a stably operating oscillator during this section. A highly stable oscillator is expensive, and therefore constitutes a disadvantage. Conversely, an unstable oscillator would make it impossible to achieve a sufficient frame length and result in a lower efficiency of channel utilization.

Figure 3 is a block diagram of a preferred embodiment of the present invention. Referring to the figure, an input split-phase signal A is entered into a differentiator circuit 11 and a split-phase signal-to-non-return to zero (SPL-NRZ) converter 14. The differentiator circuit 11 detects the varying points of the input point A, and supplies them to a phase detector 12. The phase detector 12, as will be described in detail later, phase-compares the output of differentiator 11 with the output of a selector 16, and supplies a phase error signal to a digital VCO 13 according to the delay or advance between them. The selector 16 selectively provides the phase detector 12 with a regenerated clock B having a frequency f_2 or with a signal E having a frequency f_1 which is twice the frequency f_2, in response to the output of a frame sync detector 15, which will be described presently. The VCO 13 controls the oscillating frequency f_1 according to the phase error signal. The output E having this frequency f_1 is bisected by a 1/2 frequency divider 17 into the regenerated clock B, which is intended to obtain.

Out of an NRZ signal provided by the SPL-NRZ converter 14, the frame sync detector 15 detects a frame sync signal FS, and supplies a detection signal D to the selector 16. As mentioned above, the selector 16, according to the detection signal D, selects either the output E of the VCO 13 or the output B resulting from the 1/2 frequency division of the output E, and supplies the selected one to the phase detector 12. The output B is selected during the dotting section DOT and the frame sync signal section FS, while the output E is during the data section DATA. The SPL-NRZ converter 14, like the Manchester decoder shown on page 142 of the BSTJ referenced above, can be composed of an exclusive OR circuit; a well known pattern matching circuit can be used as the frame sync signal detector 15, and the selector 16 can be readily realized by a simple combination of logical circuit.

Figures 4A to 4F are timing charts showing the operation of the circuit of Figure 3. The varying points of the split-phase signal A are phase-compared with the regenerated clock B having the frequency f_2 during the sections of dotting and the frame sync signal and with the clock E having the freqency f_1, which is twice as high as the frequency f_2, after the detection of the frame sync signal FS. It is seen that, as the object of phase comparison is switched to the clock E after the reception of the frame sync signal FS, even if "1" consecutively emerges, the varying point of the input signal A concurs with the trailing edge of the clock E. Further, even if "1" and "0" are repeated in the data section, in the absence of the varying point, the phase detector 12 will substantially perform no comparison, and accordingly no jitters will occur in the regenerated clock. Reasons for this will be apparent from the description referring to Figures 5 and 6A to 6G. Therefore, unlike the prior art, no varying point of the split-phase signal will arise 180 degrees off, so that the phase-adjusting operation can be continued even during the data section. Since the clock B, which is the intended timing signal, is provided by 1/2 frequency-division of the output E of the VCO 13, the phase of the clock B is matched to that of the input signal A from the beginning of the input signal, the dotting section, till the end of the data section.

Next will be described in detail the phase detector 12. Referring to Figure 5, the differentiator 11 provides clock terminals C of D-type flip-flops 121 and 122 with a differentiated signal F which has obtained from the input split-phase signal A. In response to the signal F, the flip-flops 121 and 122 latch the output G of the selector 16 and the inverted output $\overline{G}$, respectively. A high-level output at the terminal Q of flip-flop 121 indicates that the output G, i.e., the regenerated timing signal B is behind the timing of input signal A. Meanwhile, a high-level output at the terminal Q of flip-flop 122 indicates that the regenerated timing signal B precedes the timing of input signal A. The output I-1 and I-3 of flip-flops 121 and 122 are subject to NOR operation at a NOR gate 123 to provide a signal I-2 indicating that the regenerated timing signal B is in synchronism with the timing of input signal A. The flip-flops 121 and 122 are reset by a reset signal H which is produced from the output G by using an inverter 124, delay circuit 125 and AND gate 126.

In Figures 6A to 6G, the selected output G is behind by time T_D with respect to the timing of inputs signal A. The varying points of the signal A are detected by the differentiator to produce the signal F. This signal F samples the outputs G and $\overline{G}$ at flip-flops 121 and 122 to generate the signals I-1 and I-3, respectively. The signals I-1 and I-3 are NORed at NOR gate 123 to generate the signal I-2.

In response to the trailing edge of the output G, DVCO 13 (Figure 3) latches any one of the signals

I-1, I-2 and I-3, as indicated by small arrows in Figures 6E to 6G. Since the D-type flip-flops 121 and 122 have a somewhat delay themselves, DVCO 13 can latch one of signals I-1, I-2 and I-3, before the flip-flops are reset by the reset signal H. When DVCO 13 latches the signal I-2, it generates a signal having a frequency f_M substantially equal to twice the bit rate of input signal A. When DVCO 13 latches the signal I-1 or I-3, DVCO controls itself so as to generate a signal having a frequency f_H or f_L, respectively. It is assumed that the bit rate of input signal A is 10 k bit/sec and the stability of DVCO 13 is 10^{-4}. The frequency difference between the signal A and the output of DVCO becomes less than 1 Hz. The frequencies f_H and f_L may be set at 10.3 kHz and 9.7 kHz, respectively.

In the example shown in Figures 6A to 6G, DVCO controls itself so as to generate the frequency f_H because it latches the signal I-1 except for a time t_5. At the time t_5, DVCO controls its output frequency to coincide it with the frequency f_M. However, this frequency control substantially does not influence the output frequency of DVCO because the frequency difference between the frequency f_M, and the bit rate of signal A is less than 1 Hz. On the contrary, a frequency control according to the signal I-1 or I-3 significantly influences the outputs frequency of DVCO because the frequency f_H or f_L is sufficiently apart from the input bit rate, namely by 300 Hz.

The signal I-3 that is indicative of the advance of output G with respect to the signal A arises at a time t_1 and a time t_3 although the output G is behind the timing of the input signal A. The signal I-3, however, falls at the next varying points t_2 and t_4 prior to the next sampling point of output G. Therefore, the signal I-3 does not affect the latching operation of DVCO.

Figure 7 is a detailed block diagram of the frame sync signal detector 15. The NRZ signal C from the SPL-NRZ converter 15 is stored in a shift register 152 in synchronism with the regenerated clock B. The output of each stage of the shift register 152 is subject to exclusive-OR operation at an exclusive-OR circuit 153 with each bit of the frame sync signal stored in a memory section 151. Each output of the exclusive-OR circuit 153 is led to an OR gate 154 whose output is in turn supplied to an output inverter 155. Therefore, if a frame sync signal is contained in the NRZ signal C, the inverter 155 will output a logical "1" to set an RS flip-flop 156, and whereby a frame sync signal detection pulse D will be supplied to the terminal Q of the flip-flop 156. The flip-flop 156, which is already set, is reset by the control section (not shown) of a central processing unit (CPU) or the like. The control section may detect the end of data in the input split-phase signal, in accordance with the frame length, to generate a pulse required for resetting the flip-flop 156. In response to the resetting, the selector 16 begins to supply the output of the frequency divider 17 to the phase detector 12 to initialize the timing recovery circuit.

As hitherto described, the use of a timing recovery circuit according to the present invention makes possible proper phase adjustment of clocks even if either "1" or "0" consecutively emerges in the data section after the detection of the frame sync signal FS. Since there is no need to maintain the output of the VCO during the data section, the frame length can be extended without having to use an expensive crystal for the VCO. It is conceivable to do away with the 1/2 frequency divider and the selector 16 to extract clocks having a frequency twice as high as that of the timing signal (f_2) from the beginning of the input signal A, but this would entail the disadvantage of inviting phase uncertainty (180-degree displacement) in the 1/2 frequency-divided timing signal. Although this uncertainty can be corrected by detecting the frame sync signal FS, uncertainty would still remain in the section of the frame sync signal FS, whose detection itself would be thereby made inaccurate.

Claims

1. A timing recovery circuit comprising:

means for detecting the varying points of a split-phase signal having a pattern of the repetition of logical "1" and "0" at its beginning;

voltage-controlled oscillator means for generating a signal whose frequency is twice as high as that of the timing signal of said split-phase signal and controlling the frequency of the generated signal in response to a control signal;

frequency dividing means for dividing by two the output frequency of said voltage-controlled oscillator means;

selector means for selectively supplying the output of said voltage-controlled oscillator means and that of said frequency dividing means;

phase detector means for phase-comparing the output of said varying point detector means and that of said selector means, and supplying said voltage-controlled oscillator means with a signal indicating the relative delay or advance between the two outputs as said control signal; and

control means for controlling said selector means so that it selects the output of said frequency dividing means during said repetitive pattern of logical "1" and "0" and that of said voltage-controlled oscillator means elsewhere.

2. A timing recovery circuit, as claimed in Claim 1, wherein said split-phase signal includes a frame synchronization signal after said repetitive pattern, and wherein said control means comprises converter means responsive to the output of said frequency divider means for converting said split-phase signal into a non-return to zero signal, and frame synchronization signal detector means for detecting said frame synchronization signal and supplying a detection signal for distinguishing between the section of said repetitive pattern and other sections.

3. A timing recovery circuit, as claimed in Claim 2, wherein said frame synchronization signal detector means comprises pattern matching

I-1, I-2 and I-3, as indicated by small arrows in Figures 6E to 6G. Since the D-type flip-flops 121 and 122 have a somewhat delay themselves, DVCO 13 can latch one of signals I-1, I-2 and I-3, before the flip-flops are reset by the reset signal H. When DVCO 13 latches the signal I-2, it generates a signal having a frequency f_M substantially equal to twice the bit rate of input signal A. When DVCO 13 latches the signal I-1 or I-3, DVCO controls itself so as to generate a signal having a frequency f_H or f_L, respectively. It is assumed that the bit rate of input signal A is 10 k bit/sec and the stability of DVCO 13 is 10^{-4}. The frequency difference between the signal A and the output of DVCO becomes less than 1 Hz. The frequencies f_H and f_L may be set at 10.3 kHz and 9.7 kHz, respectively.

In the example shown in Figures 6A to 6G, DVCO controls itself so as to generate the frequency f_H because it latches the signal I-1 except for a time t_5. At the time t_5, DVCO controls its output frequency to coincide it with the frequency f_M. However, this frequency control substantially does not influence the output frequency of DVCO because the frequency difference between the frequency f_M, and the bit rate of signal A is less than 1 Hz. On the contrary, a frequency control according to the signal I-1 or I-3 significantly influences the outputs frequency of DVCO because the frequency f_H or f_L is sufficiently apart from the input bit rate, namely by 300 Hz.

The signal I-3 that is indicative of the advance of output G with respect to the signal A arises at a time t_1 and a time t_3 although the output G is behind the timing of the input signal A. The signal I-3, however, falls at the next varying points t_2 and t_4 prior to the next sampling point of output G. Therefore, the signal I-3 does not affect the latching operation of DVCO.

Figure 7 is a detailed block diagram of the frame sync signal detector 15. The NRZ signal C from the SPL-NRZ converter 15 is stored in a shift register 152 in synchronism with the regenerated clock B. The output of each stage of the shift register 152 is subject to exclusive-OR operation at an exclusive-OR circuit 153 with each bit of the frame sync signal stored in a memory section 151. Each output of the exclusive-OR circuit 153 is led to an OR gate 154 whose output is in turn supplied to an output inverter 155. Therefore, if a frame sync signal is contained in the NRZ signal C, the inverter 155 will output a logical "1" to set an RS flip-flop 156, and whereby a frame sync signal detection pulse D will be supplied to the terminal Q of the flip-flop 156. The flip-flop 156, which is already set, is reset by the control section (not shown) of a central processing unit (CPU) or the like. The control section may detect the end of data in the input split-phase signal, in accordance with the frame length, to generate a pulse required for resetting the flip-flop 156. In response to the resetting, the selector 16 begins to supply the output of the frequency divider 17 to the phase detector 12 to initialize the timing recovery circuit.

As hitherto described, the use of a timing recovery circuit according to the present invention makes possible proper phase adjustment of clocks even if either "1" or "0" consecutively emerges in the data section after the detection of the frame sync signal FS. Since there is no need to maintain the output of the VCO during the data section, the frame length can be extended without having to use an expensive crystal for the VCO. It is conceivable to do away with the 1/2 frequency divider and the selector 16 to extract clocks having a frequency twice as high as that of the timing signal (f_2) from the beginning of the input signal A, but this would entail the disadvantage of inviting phase uncertainty (180-degree displacement) in the 1/2 frequency-divided timing signal. Although this uncertainty can be corrected by detecting the frame sync signal FS, uncertainty would still remain in the section of the frame sync signal FS, whose detection itself would be thereby made inaccurate.

Claims

1. A timing recovery circuit comprising:

means for detecting the varying points of a split-phase signal having a pattern of the repetition of logical "1" and "0" at its beginning;

voltage-controlled oscillator means for generating a signal whose frequency is twice as high as that of the timing signal of said split-phase signal and controlling the frequency of the generated signal in response to a control signal;

frequency dividing means for dividing by two the output frequency of said voltage-controlled oscillator means;

selector means for selectively supplying the output of said voltage-controlled oscillator means and that of said frequency dividing means;

phase detector means for phase-comparing the output of said varying point detector means and that of said selector means, and supplying said voltage-controlled oscillator means with a signal indicating the relative delay or advance between the two outputs as said control signal; and

control means for controlling said selector means so that it selects the output of said frequency dividing means during said repetitive pattern of logical "1" and "0" and that of said voltage-controlled oscillator means elsewhere.

2. A timing recovery circuit, as claimed in Claim 1, wherein said split-phase signal includes a frame synchronization signal after said repetitive pattern, and wherein said control means comprises converter means responsive to the output of said frequency divider means for converting said split-phase signal into a non-return to zero signal, and frame synchronization signal detector means for detecting said frame synchronization signal and supplying a detection signal for distinguishing between the section of said repetitive pattern and other sections.

3. A timing recovery circuit, as claimed in Claim 2, wherein said frame synchronization signal detector means comprises pattern matching

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means for matching the pattern of said non-return to zero signal and that of said frame synchronization signal, and flip-flop means being set by the output of said pattern matching means and reset by a signal obtained in response to the completion of the other sections of said split-phase signal, for supplying its output to said selector means.

4. A timing recovery circuit, as claimed in Claim 2 or 3, wherein said converter means comprises exclusive OR means for taking the exclusive OR of said split-phase signal and the output of said frequency divider means to produce said non-return to zero signal.

Patentansprüche

1. Taktwiedergewinnungsschaltung mit

einer Einrichtung zum Detektieren der Variationspunkte eines Spaltphasensignals mit einem Wiederholungsmuster bestehend aus logisch "1" und "0" am Anfang;

einem spannungsgesteuerten Oszillator zum Erzeugen eines Signals, dessen Frequenz doppelt so hoch ist wie die des Taktsignals des Spaltphasensignals und zum Regeln der Frequenz des erzeugten Signals in Abhängigkeit vom Steuersignal;

einer Frequenzdividiereinrichtung zum Teilen der Ausgangsfrequenz des spannungsgesteuerten Oszillators um den Faktor zwei;

einer Wähleinrichtung zum wahlweisen Zuführen des Ausgangssignals des spannungsgesteuerten Oszillators und des Ausgangssignals der Frequenzdividiereinrichtung;

einem Phasendetektor zum Phasenvergleich des Ausgangssignals des Variationspunktdetektors und des Ausgangssignals der Wähleinrichtung sowie Zuführen eines Signals, das die relative Vorzögerung oder Voreilung der zwei Ausgangssignale wiedergibt, als Steuersignal zu dem spannungsgesteuerten Oszillator; und

einer Steuereinrichtung zum Steuern der Wähleinrichtung, so daß das Ausgangssignal der Frequenzdividiereinrichtung während des Wiederholungsmusters mit logisch "1" und "0" sowie das Ausgangssignal des spannungsgesteuerten Oszillators ausgewählt wird.

2. Taktwiedergewinnungsschaltung nach Anspruch 1, dadurch gekennzeichnet, daß das Spaltphasensignal nach dem Wiederholmuster ein Rahmensynchronisationssignal aufweist, daß die Steuereinrichtung einen Wandler aufweist, der auf das Ausgangssignal der Frequenzteilereinrichtung anspricht, um das Spaltphasensignal in ein Signal ohne Rückkehr zu Null umzuwandeln, und daß ein Rahmensynchronisationssignaldetektor vorgesehen ist, um das Rahmensynchronisationssignal festzustellen und ein Detektionssignal zur Unterscheidung zwischen dem Abschnitt des Wiederholmusters und anderen Abschnitten zu erzeugen.

3. Taktwiedergewinnungsschaltung nach Anspruch 2, dadurch gekennzeichnet, daß der Rahmensynchronisationssignaldetektor eine Mustererkennungseinrichtung aufweist, um das Muster des Signals ohne Rückkehr zu Null und das des Rahmensynchronisationssignals anzupassen, und daß eine Flip-Flop-Einrichtung durch das Ausgangssignal der Musterekennungseinrichtung gesetzt und durch ein beim Abschluß der anderen Abschnitte des Spaltphasensignals erhaltenen Signal auf "0" zurückgesetzt wird, um ihr Ausgangssignal der Wähleinrichtung zuzuführen.

4. Taktwiedergewinnungsschaltung nach Anspruch 2 oder 3, dadurch gekennzeichnet, daß der Wandler eine Exklusiv-ODER-Einrichtung aufweist, um das Spaltphasensignal und das Ausgangssignal der Frequenzdividiereinrichtung einer Exklusiv-ODER-Prüfung zu unterwerfen, um das Signal ohne Rückkehr zu Null zu erzeugen.

Revendications

1. Circuit de récupération d'horloge comprenant:

un moyen pour détecter les points variables d'un signal à phase auxiliaire ayant un profil de la répétition des logiques "1" et "0" à son commencement;

un moyen d'oscillator piloté par tension pour produire un signal dont la fréquence est le double de celle du signal d'horloge du signal à phase auxiliaire et commander la fréquence du signal généré en réponse à un signal de commande;

un moyen de division de la fréquence afin de diviser par deux la fréquence de sortie de l'oscillateur piloté par tension;

un moyen de sélecteur pour fournir sélectivement la sortie du moyen d'oscillateur piloté par tension et celle du moyen de division de la fréquence;

un moyen de détecteur de phase pour comparer en phase la sortie du moyen de détecteur du points variables et celle du moyen de sélecteur, et fournir au moyen d'oscillateur piloté par tension un signal indiquant le retard ou l'avance relatifs entre les deux sorties comme signal de commande; et

un moyen de commande pour commander le moyen de sélecteur de façon qu'il sélectionne la sortie du moyen de division de la fréquence pendant le profil répétitif des niveau logiques "1" et "0" et celle du moyen d'scillateur piloté par tension.

2. Circuit de récupération d'horloge selon la revendication 1, dans lequel le signal à phase auxiliaire comporte un signal de synchronisation de trame après le profile répétitif, et dans lequel le moyen de commande comprend un moyen de convertisseur répondant à la sortie du moyen diviseur de fréquence pour convertir le signal à phase auxiliaire en un signal de non-retour à zéro, et un moyen de détecteur du signal de synchronisation de trame pour détecter le signal de synchronisation de trame et fournir un signal de détection pour faire la distinction entre la section du profil répétitif et d'autres sections.

3. Circuit de récupération d'horloge selon la

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revendication 2, dans lequel le moyen de détecteur du signal de synchronisation de trame comprend un moyen d'adaptation de profil afin d'adapter le profil du signal de non-retour à zéro et celui du signal de synchronisation de trame, et un moyen de bascule étant chargé par la sortie du moyen d'adaptation de profil et remis à zéro par un signal obtenu en réponse à l'achèvement des autres sections du signal à phase auxiliaire, afin de fournir sa sortie au moyen de sélecteur.

4. Circuit de récupération d'horloge selon la revendication 2 ou la revendication 3, dans lequel le moyen de convertisseur comprend un moyen OU Exclusif pour prendre le OU Exclusif du signal à phase auxiliaire et la sortie du moyen diviseur de fréquence afin de produire le signal de non retour à zéro.

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