

Description

The present invention relates to a passive optical network, and in particular to a head-end station for use in such a network.

The present applicant has developed a bit transport system (BTS) for use in a TPON (telephony on a passive optical network) network. In this bit transport system a head-end station broadcasts time division multiple access (TDMA) frames to all the terminations on the network. The transmitted frames include both traffic data and control data. Each termination recognises and responds to an appropriately addressed portion of the data in the broadcast frame and ignores the remainder of the frame.

In the upstream direction, each termination transmits data in a predetermined time slot and the data from the different terminations are assembled at the head-end into a TDMA frame of predetermined format.

Typically each TDMA frame includes a header containing bits relating to system functions such as coarse or fine ranging followed by a number of basic frames carrying the traffic data. In the preferred embodiment described below, each basic frame is 2496 bits long, comprising 2352 traffic bits followed by 144 control bits. The control bits may be used by the head-end station, for example, to control the timing and amplitude of the transmissions from the terminations on the network. The appropriate control data is generated by a CPU within the head-end station. On the transmit side of the head-end station it is therefore necessary to assemble the control and traffic data from different sources to form the basic frames. A corresponding function is required for the return data, with it being necessary to split the received frames into traffic and control data.

Typically prior art arrangements are described in EP-A-253381, US-A-4498169 and US-A-4823312. EP-A-253 381 discloses a head-end station according to the preamble of Claim 1, while US-A-4 498 169 describes a head-end station as defined in the preamble of Claim 6.

The present invention provides a head-end station for a passive optical network system arranged to transmit downstream TDMA frames and to receive upstream TDMA frames, each TDMA frame including a plurality of basic frames, each basic frame comprising a plurality of traffic bits and a plurality of control bits, the head-end station including a data receiver comprising a control processor arranged to receive control data, a control data buffer arranged to provide a parallel control data input to the control processor, a traffic interface for receiving traffic data, and a serial-to-parallel converter for receiving incoming TDMA frames, characterised in that the serial-to-parallel converter broadcasts said frames to the control data buffer and to the traffic interface, the control data re-

ceived by the control data buffer corresponding to the control data portion of a received basic frame, and the traffic data received by the traffic interface corresponding to the traffic data portion of a received basic frame, and characterised by synchronising means for synchronising the control data buffer and the traffic interface to the overall frame structure, for timing the control data buffer so that only the control portion of each basic frame is input thereto, and for timing the traffic interface so that only the traffic portion of each basic frame is input thereto.

The present invention thus provides a structure for the data receivers and transmitters within the head-end station which is ideally adapted to the interleaving of control and traffic data within the TDMA frame, and enables the use of such frame structures without requiring complex multiplexers or de-multiplexers. In the past, the use of such multiplexers or de-multiplexers in the input and output stages has provided a bottleneck which seriously restricted the performance of the system.

Typically, the traffic interface is an exchange interface handling telephone traffic.

Preferably, each of the upstream TDMA frames includes a header preceding the plurality of basic frames, and the control data buffer reads control data from the serial-to-parallel converter both during the header and subsequently during the portions of the basic frames comprising the control bits. Preferably, the header includes a phase-1 ranging portion, and the control data buffer is arranged to capture any ranging pulses received in the phase-1 ranging portion.

This structure is found to be particularly advantageous when the frames include a header used for system control functions as well as the control bits associated with each of the basic frames. The present invention makes it possible to capture and process both these forms of data using the same hardware, thereby reducing the cost of that hardware and further simplifying the control procedures. It is found to be particularly advantageous when the header includes phase-1 ranging pulses, since it is then possible to capture and process those pulses without requiring additional hardware.

Phase-1 ranging pulses are used for coarse adjustment of the timing transmissions from the terminations to compensate for their different loop delays. This is described in further detail in EP-B-495855.

Preferably, the control data buffer comprises a pair of memory buffers connected in parallel between the serial-to-parallel converter and respective inputs of the control processor, so that when one of the memory buffers is being written to by the serial-to-parallel converter, the control processor reads data from the other of the memory buffers. Preferably, the memory buffers are video line memory buffers.

The invention also provides a head-end station

for a passive optical network system arranged to transmit downstream TDMA frames and to receive upstream TDMA frames, each TDMA frame including a plurality of basic frames, each basic frame comprising a plurality of traffic bits and a plurality of control bits, the head-end station including a data transmitter comprising a control processor arranged to transmit control data, a control data buffer arranged to receive a parallel control data stream from the control processor, a traffic interface arranged to transmit to traffic data, and a parallel-to-serial converter arranged to transmit outgoing TDMA frames, characterised in that the outputs of the control data buffer and the traffic interface are connected in parallel as input to the parallel-to-serial converter to provide the appropriate control and traffic portions of a basic frame, the control data provided by the control data buffer corresponding to the control data portion of a transmitted basic frame, and the traffic data provided by the traffic interface corresponding to the traffic data portion of a transmitted basic frame, and characterised by synchronising means for synchronising the control data buffer and the traffic interface to the overall frame structure, for timing the control data buffer so that only the control portion of each basic frame is output therefrom, and for timing the traffic interface so that only the traffic portion of each basic frame is output therefrom.

Preferably, each of the downstream TDMA frames includes a header preceding the plurality of basic frames, and the control data buffer writes control data to the parallel-to-serial converter both during the header and subsequently during the portions of the basic frames comprising the control bits.

Preferably, the header includes a system diagnostic portion, and the control data buffer is arranged to output system diagnostic pulses in the system diagnostic portion.

Just as on the receive side, it is found to be particularly advantageous to use a control data buffer both for the control portions of the basic frames and for the header, so similar advantages arise from the use of an analogous structure on the transmit side. The header in each of the downstream frames may include pulses which are transmitted onto the network in order to monitor the state of the network. In particular, these systems diagnostic pulses may take the form of an optical time domain reflectometry (OTDR) probe, formed from encoded pulses having an appropriate autocorrelation function. The transmission of such pulses makes it possible, for example, to detect faults in the fibre optic network.

Preferably, the control data buffer comprises a pair of memory buffers connected in parallel between the parallel-to-serial converter and respective outputs of the control processor, so that when one of the memory buffers is writing data to the parallel-to-serial converter, the control processor writes data to the

other of the memory buffers. Preferably, the memory buffers are video line memory buffers.

A head-end station constructed in accordance with the invention will now be described in detail, by way of example, with reference to the accompanying drawings, in which:-

Figure 1A is a block diagram showing a TPON network;

Figure 1B is a diagram showing the structure of an upstream TDMA frame;

Figure 2 is a block diagram of a head-end station;

Figure 3 is a block diagram of a data receiver stage;

Figure 4 is a block diagram of a data transmitter stage; and

Figure 5a-5g are timing diagrams for the circuits of Figures 3 and 4.

Figure 1A shows a TPON network comprising a head-end station 1, a number of terminations 2, and a passive optical fibre network 3 linking the head-end station to the terminations. Although, for clarity, only three terminations 2 are shown, in practice many more terminations will be connected to the single head-end station 1. Typically, the head-end station 1 is located in a local telephone exchange, and the terminations 2 are subscriber stations in domestic or commercial premises or street cabinets in the neighbourhood of the local exchange.

The head-end station 1 broadcasts data over the fibre network 3 as time division multiple access (TDMA) frames having a predetermined format. The frames include control channels addressed to specific ones of the terminations 2 to control, amongst other parameters, the amplitude and timing of the optical signals transmitted onto the fibre network 3 by the terminations 2.

In the upstream direction, each termination 2 transmits data in a predetermined time slot, which data is assembled into a TDMA frame at the head-end station 1. Since the TPON network is synchronous in operation it is necessary to control the timing of the terminations both to compensate for the different delays associated with different positions of the terminations on the fibre network 3 and to correct for any variation in the delay and amplitude arising, for example, from local fluctuations in the temperature of the network.

Figure 1B shows the format of the return frame. Traffic data is transmitted to the head-end station in 80 basic frames BF1... BF80. The basic frames BF1... BF80 are preceded by a header H which includes a phase-2 ranging section R 720 bits long. Each termination 2 is arranged to transmit onto the fibre network 3 a ranging bit timed to arrive at a predetermined position within the ranging section R. The head-end station 1 determines the phase of each arriving ranging pulse and then transmits control signals to the respective termination 2 to retard or advance the timing

of the transmission from that termination 2 in order to minimise the phase offset between the received data from that termination and the intended position of that data within the return frame structure.

Figure 2 shows the structure of the head-end station 1. The incoming optical signals are received by an input stage 4 which includes a conventional photo-electric detector. The output from the input stage 4 is branched, going both to a signal recovery stage 5 and to an A/D sampler 6. The sampler 6 operates under the control of the main CPU 7 to sample any selected portion of the incoming signals. The output from the sampler 6 is changed to a datastream of longer word-length and lower bit-rate by a converter 8. The use of the sampler 6 is described in greater detail in EP-A-502004.

The signal recovery stage includes a data receiver as shown in greater detail in Figure 3.

The serial data input stream is applied to a serial-to-parallel converter 11. The output from the serial-to-parallel converter 11 is communicated via an 8-bit wide data bus at a data rate of 2.56 Mbit/s.

In order to prevent read/write conflicts, two dual port parallel line memory buffers (video line memories) 13, 14 are provided for the control processor 12 which has DMA access to both of the buffers. When data is being written from the converter 11 to a given one of the buffers 13, 14, then a flag is set so that the processor reads from the other of the buffers 14, 13.

An exchange interface 15 is provided comprising an 8-bit wide FIFO arranged to provide eight parallel exchange traffic output streams T1 T8.

In use, each incoming basic frame BF is broadcast both to the control processor buffers 13, 14 and to the exchange interface 15. The operation of the buffers 13, 14 and the interface 15 is synchronised to the overall frame structure, and timed so that the control buffers read only the control portion of each basic frame, and the exchange interface 15 reads only the traffic portion. The appropriate enable signals are generated by a timing unit locked to the exchange clock.

On the transmit side of the head-end station, a corresponding structure, shown in Figure 4, is used. Control data from a control processor 12' are fed via buffers 13', 14' onto a parallel 8-bit bus. Traffic data is fed onto the bus from an exchange interface 15'. On the output side of the bus a parallel-to-serial converter 11' forms a serial data stream. As on the receiver side, the timing of the control processor buffers 13', 14' and the exchange interface 15' is synchronised to provide traffic and control data in the appropriate portions of each outgoing basic frame BF. The bit order of the output frame is scrambled using a scrambler S. A suitable scrambler is described in EP-B-318335.

Figures 5a-5g show timing diagrams for the enable signals to the control buffers and the exchange

interface. Figure 5a shows the CPU interrupt which has the same 10ms period as the received TDMA frames. Figure 5b shows the time of the bank switch which switches alternately between the two video line memories of the data buffer in the transmitter under the control of the timing unit. Figure 5c shows the enabling signal for the buffer: the signal enables when it is low. It is timed first to go low during the part of the header corresponding to the phase-1 ranging period. Subsequently, the buffer is enabled towards the end of each basic frame in order to capture the control data associated with that basic frame. As shown in Figure 5d, the enable signal for the other of the video line memories has the same structure but with a shift in phase of one frame's length. The header is used for system diagnostics. An encoded signal is transmitted onto the fibre network and the state of the network may be analysed using OTDR techniques.

Figures 5e-5g show the timing of the data receiver. The structure is generally analogous to that used on the transmit side, but with a phase offset of 250 microseconds corresponding to the loop delay for the entire network system. The receive buffers when enabled in the header portion capture phase-1 pulses, for use in controlling the timing of transmissions from the terminations, as described above.

Claims

1. A head-end station for a passive optical network system arranged to transmit downstream TDMA frames and to receive upstream TDMA frames, each TDMA frame including a plurality of basic frames, each basic frame comprising a plurality of traffic bits and a plurality of control bits, the head-end station including a data receiver (5) comprising a control processor (12) arranged to receive control data, a control data buffer (13, 14) arranged to provide a parallel control data input to the control processor, a traffic interface (15) for receiving traffic data, and a serial-to-parallel converter (11) for receiving incoming TDMA frames, characterised in that the serial-to-parallel converter is arranged to broadcast said frames to the control data buffer and to the traffic interface, the control data received by the control data buffer corresponding to the control data portion of a received basic frame, and the traffic data received by the traffic interface corresponding to the traffic data portion of a received basic frame, and in that the data receiver further comprises synchronising means for synchronising the control data buffer and the traffic interface to the overall frame structure, for timing the control data buffer so that only the control portion of each basic frame is input thereto, and for timing the



of the transmission from that termination 2 in order to minimise the phase offset between the received data from that termination and the intended position of that data within the return frame structure.

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Claims

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traffic interface so that only the traffic portion of each basic frame is input thereto.

2. A head-end station according to claim 1, in which each of the upstream TDMA frames includes a header preceding the plurality of basic frames, and the control data buffer (13, 14) is arranged to read control data from the serial-to-parallel converter (11) both during the header and subsequently during the portions of the basic frames comprising the control bits. 5
3. A head-end station according to claim 1 or claim 2, in which the header includes a phase-1 ranging portion, and the control data buffer (13, 14) is arranged to capture ranging pulses received during the phase-1 ranging portion. 10
4. A head-end station according to any one of the preceding claims, in which the control data buffer comprises a pair of memory buffers (13, 14) connected in parallel between the serial-to-parallel converter (11) and respective inputs of the control processor (12), so that when one of the memory buffers is being written to by the serial-to-parallel converter, the control processor reads data from the other of the memory buffers. 15
5. A head-end station according to claim 4, in which the memory buffers (13, 14) are video line memory buffers. 20
6. A head-end station for a passive optical network system arranged to transmit downstream TDMA frames and to receive upstream TDMA frames, each TDMA frame including a plurality of basic frames, each basic frame comprising a plurality of traffic bits and a plurality of control bits, the head-end station including a data transmitter comprising a control processor (12') arranged to transmit control data, a control data buffer (13', 14') arranged to receive a parallel control data stream from the control processor, a traffic interface (15') arranged to transmit to traffic data, and a parallel-to-serial converter (11') arranged to transmit outgoing TDMA frames, characterised in that the outputs of the control data buffer and the traffic interface are connected in parallel as input to the parallel-to-serial converter to provide the appropriate control and traffic portions of a basic frame, the control data provided by the control data buffer corresponding to the control data portion of a transmitted basic frame, and the traffic data provided by the traffic interface corresponding to the traffic data portion of a transmitted basic frame, and in that the data transmitter further comprises synchronising means for synchronising the control data buffer and the traffic inter-

face to the overall frame structure, for timing the control data buffer so that only the control portion of each basic frame is output therefrom, and for timing the traffic interface so that only the traffic portion of each basic frame is output therefrom.

7. A head-end station according to claim 6, in which each of the downstream TDMA frames includes a header preceding the plurality of basic frames, and the control data buffer (13', 14') writes control data to the parallel-to-serial converter (11') both during the header and subsequently during the portions of the basic frames comprising the control bits. 25
8. A head-end station according to claim 7, in which the header includes a system diagnostic portion, and the control data buffer (13', 14') is arranged to output system diagnostic pulses in the system diagnostic portion. 30
9. A head-end station according to any one of claims 6 to 8, in which the control data buffer comprises a pair of memory buffers (13', 14') connected in parallel between the parallel-to-serial converter (11') and respective outputs of the control processor (12'), so that when one of the memory buffers is writing data to the parallel-to-serial converter (11'), the control processor writes data to the other of the memory buffers. 35
10. A head-end station according to claim 9, in which the memory buffers (13', 14') are video line memory buffers. 40

Patentansprüche

1. Empfangsstellen-Apparat für ein passives optisches Netzwerksystem, daß vorgesehen ist, um stromabwärtige TDMA-Rahmen zu übertragen und um stromaufwärtige TDMA-Rahmen zu empfangen, wobei jeder TDMA-Rahmen eine Mehrzahl von Grundrahmen enthält, wobei jeder Grundrahmen eine Mehrzahl von Verkehrsbits und eine Mehrzahl von Steuerbits enthält, wobei der Empfangsstellen-Apparat einen Datenempfänger (5) enthält, der versehen ist mit: einem Steuerungsprozessor (12), der vorgesehen ist, um Steuerdaten zu empfangen, einem Steuerdatenpuffer (13, 14), der vorgesehen ist, um einen parallelen Steuerdateneingang zu dem Steuerungsprozessor zu schaffen, einer Verkehrschnittstelle (15) zum Empfangen von Verkehrsdaten, und einem Seriell/Parallel-Wandler (11) zum Empfangen eingehender TDMA-Rahmen, dadurch gekennzeichnet, daß der Seriell/Parallel-Wandler vorgesehen ist, um die Rahmen zu



- dem Steuerdatenpuffer und der Verkehrsschnittstelle zu senden, wobei die von dem Steuerdatenpuffer empfangenen Steuerdaten dem Steuerdatenabschnitt eines empfangenen Grundrahmens entsprechen, und die von der Verkehrsschnittstelle empfangenen Verkehrsdaten dem Verkehrsdatenabschnitt eines empfangenen Grundrahmens entsprechen, und daß der Datenempfänger weiterhin versehen ist mit einer Synchronisierereinrichtung zum Synchronisieren des Steuerdatenpuffers und der Verkehrsschnittstelle mit der allgemeinen Rahmenstruktur, zum Takten des Steuerdatenpuffers, so daß nur der Steuerabschnitt eines jeden Grundrahmens in ihn eingegeben wird, und zum Takten der Verkehrsschnittstelle, so daß nur der Verkehrsabschnitt eines jeden Grundrahmens in ihn eingegeben wird.
2. Empfangsstellen-Apparat nach Anspruch 1, in dem jeder der stromaufwärtigen TDMA-Rahmen einen Anfangsblock enthält, der der Mehrzahl von Grundrahmen vorläuft, und der Steuerdatenpuffer (13, 14) vorgesehen ist, um Steuerdaten aus dem Seriell/Parallel-Wandler (11) sowohl während des Anfangsblocks als auch anschließend während der Abschnitte der Grundrahmen, die die Steuerbits enthalten, zu lesen.
 3. Empfangsstellen-Apparat nach einem der Ansprüche 1 oder 2, in dem der Anfangsblock einen Phase-1 Bereichsabschnitt enthält, und der Steuerdatenpuffer (13, 14) vorgesehen ist, um Bereichsimpulse einzufangen, die während des Phase-I Bereichsabschnitts empfangen wurden.
 4. Empfangsstellen-Apparat nach einem der vorhergehenden Ansprüche, in dem der Datenpuffer ein Paar von Speicherpuffern (13, 14) enthält, die parallel zwischen dem Seriell/Parallel-Wandler (11) und entsprechenden Eingängen des Steuerungsprozessors (12) verbunden sind, so daß der Steuerungsprozessor Daten von dem anderen der Speicherpuffer liest, wenn der erste der Speicherpuffer von dem Seriell/Parallel-Wandler beschrieben wird.
 5. Empfangsstellen-Apparat nach Anspruch 4, in dem die Speicherpuffer (13, 14) Speicherpuffer für Videoleitungen sind.
 6. Empfangsstellen-Apparat für ein passives optisches Netzwerksystem, das vorgesehen ist, um stromabwärtige TDMA-Rahmen zu übertragen und stromaufwärtige TDMA-Rahmen zu empfangen, wobei jeder TDMA-Rahmen eine Mehrzahl von Grundrahmen enthält, wobei jeder Grundrahmen eine Mehrzahl von Steuerbits und eine

Mehrzahl von Steuerbits enthält, wobei der Empfangsstellen-Apparat eine Datenübertragungseinheit aufweist, die versehen ist mit einem Steuerungsprozessor (12'), der vorgesehen ist, um Steuerdaten zu übertragen, einem Steuerdatenpuffer (13', 14'), der vorgesehen ist, um einen parallelen Steuerdatenstrom von dem Steuerungsprozessor zu empfangen, einer Verkehrsschnittstelle (15'), die vorgesehen ist, um Verkehrsdaten zu übertragen, und einem Parallel/Seriell-Wandler (11'), der vorgesehen ist, um ausgehende TDMA-Rahmen zu übertragen, dadurch gekennzeichnet, daß Ausgänge des Steuerdatenpuffers und der Verkehrsschnittstelle parallel verbunden sind, als Eingang in den Parallel/Seriell-Wandler, um die geeigneten Steuer- und Verkehrsabschnitte eines Grundrahmens zu liefern, wobei die von dem Steuerdatenpuffer gelieferten Steuerdaten dem Steuerdatenabschnitt eines übertragenden Grundrahmens entsprechen, und die von der Verkehrsschnittstelle gelieferten Verkehrsdaten dem Verkehrsdatenabschnitt eines übertragenden Grundrahmens entsprechen, und daß die Datenübertragungseinheit des weiteren versehen ist mit einer Synchronisierereinrichtung zum Synchronisieren des Steuerdatenpuffers und der Verkehrsschnittstelle mit der allgemeinen Rahmenstruktur, zum Takten des Steuerdatenpuffers derart, daß nur der Steuerabschnitt eines jeden Grundrahmens aus ihr ausgegeben wird, und zum Takten der Verkehrsschnittstelle, so daß nur der Verkehrsabschnitt eines jeden Grundrahmens aus ihr ausgegeben wird.

7. Empfangsstellen-Apparat nach Anspruch 6, in dem jeder der stromabwärtigen TDMA-Rahmen einen Anfangsblock enthält, der der Mehrzahl von Grundrahmen vorläuft, und in dem der Steuerdatenpuffer (13', 14') Steuerdaten in den Parallel/Seriell-Wandler (11') sowohl während des Anfangsblocks als auch anschließend während der Abschnitte der Grundrahmen, die die Steuerbits enthalten, einschreibt.
8. Empfangsstellen-Apparat nach Anspruch 7, in dem der Anfangsblock einen Systemdiagnoseabschnitt enthält, und der Steuerdatenpuffer (13', 14') vorgesehen ist, um Systemdiagnoseimpulse in dem Systemdiagnoseabschnitt auszugeben.
9. Empfangsstellen-Apparat nach einem der Ansprüche 6 bis 8, in dem der Steuerdatenpuffer ein Paar von Speicherpuffern (13', 14') enthält, die parallel zwischen dem Parallel/Seriell-Wandler (11') und entsprechenden Ausgängen des Steuerungsprozessors (12') verbunden sind, so daß der Steuerungsprozessor Daten in den anderen



der Speicherpuffer einschreibt, wenn der erste der Speicherpuffer Daten in den Parallel/Seriell-Wandler (11') einschreibt.

10. Empfangsstellen-Apparat nach Anspruch 9, in dem die Speicherpuffer (13', 14') Speicherpuffer für Videoleitungen sind.

Revendications

1. Station tête de réseau destinée à un système de réseau optique passif agencé afin d'émettre des trames TDMA aval et à recevoir des trames TDMA amont, chaque trame TDMA comprenant une pluralité de trames de base, chaque trame de base comprenant une pluralité de bits de trafic et une pluralité de bits de commande, la station tête de réseau comportant un récepteur de données (5) comprenant un processeur de commande (12) agencé pour recevoir des données de commande, une mémoire tampon de données de commande (13, 14) agencée pour procurer une entrée de données de commande parallèle au processeur de commande, une interface de trafic (15) destinée à recevoir des données de trafic, et un convertisseur série/parallèle (11) destiné à recevoir les trames TDMA entrantes, caractérisé en ce que le convertisseur série/parallèle est agencé pour diffuser lesdites trames vers la mémoire tampon de données de commande et vers l'interface de trafic, les données de commande reçues par la mémoire tampon de données de commande correspondant à la partie données de commande d'une trame de base reçue, et les données de trafic reçues par l'interface de trafic correspondant à la partie de données de trafic d'une trame de base reçue, et en ce que le récepteur de données comprend en outre un moyen de synchronisation destiné à synchroniser la mémoire tampon de données de commande et l'interface de trafic avec la structure de trame globale, afin de synchroniser la mémoire tampon de données de commande de façon à ce que seule la partie de commande de chaque trame de base soit entrée dans celle-ci, et afin de synchroniser l'interface de façon à ce que seule la partie de trafic de chaque trame de base soit entrée dans celle-ci.
2. Station tête de réseau selon la revendication 1, dans laquelle chacune des trames TDMA amont comprend un en-tête précédent la pluralité des trames de base, et la mémoire tampon de données de commande (13, 14) est agencée pour lire les données de commande à partir du convertisseur série/parallèle (11) à la fois pendant l'en-tête et ultérieurement pendant les parties des trames

de base comprenant les bits de commande.

3. Station tête de réseau selon la revendication 1 ou la revendication 2, dans laquelle l'en-tête comprend une partie de mesure de distance de phase-1, et la mémoire tampon de données de commande (13, 14) est agencée pour capturer les impulsions de mesure de distance reçues pendant la partie de mesure de distance de phase-1.
4. Station tête de réseau selon l'une quelconque des revendications précédentes, dans laquelle la mémoire tampon de données de commande est constituée d'une paire de tampons mémoire (13, 14) reliés en parallèle entre le convertisseur série/parallèle (11) et les entrées respectives du processeur de commande (12), de façon à ce que lorsqu'un des tampons mémoire reçoit une écriture du convertisseur série/parallèle, le processeur de commande lise les données à partir de l'autre des tampons mémoire.
5. Station tête de réseau selon la revendication 4, dans laquelle les tampons mémoire (13, 14) sont des tampons mémoire de ligne vidéo.
6. Station tête de réseau destiné à un système de réseau optique passif agencé afin d'émettre des trames TDMA aval et recevoir des trames TDMA amont, chaque trame TDMA comprenant une pluralité de trames de base, chaque trame de base comprenant une pluralité de bits de trafic et une pluralité de bits de commande, la station tête de réseau comprenant un émetteur de données constitué d'un processeur de commande (12') agencé afin d'émettre les données de commande, une mémoire tampon de données de commande (13', 14') agencée afin de recevoir un flux de données de commande parallèle provenant du processeur de commande, une interface de trafic (15') agencée afin d'émettre des données de trafic, et un convertisseur parallèle/série (11') agencé afin d'émettre des trames TDMA sortantes, caractérisée en ce que les sorties de la mémoire tampon de données de commande et de l'interface de trafic sont reliés en parallèle en tant qu'entrée du convertisseur parallèle/série afin de procurer la commande appropriée et les parties de trafic d'une trame de base, les données de commande procurées par la mémoire tampon de données de commande correspondant à la partie de données de commande d'une trame de base émise, et les données de trafic procurées par l'interface de trafic correspondant à la partie de données de trafic d'une trame de base émise, et en ce que l'émetteur de données comprend en outre un moyen de synchronisation



destiné à synchroniser la mémoire tampon de données de commande et l'interface de trafic avec la structure de trame globale afin de synchroniser la mémoire tampon de données de commande de façon à ce que seule la partie de commande de chaque trame de base soit sortie de celle-ci, et afin de synchroniser l'interface de trafic de façon à ce que seule la partie de trafic de chaque trame de base soit sortie de celle-ci.

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7. Station tête de réseau selon la revendication 6, dans laquelle chacune des trames TDMA aval comprend un en-tête précédant la pluralité des trames de base, et la mémoire tampon de données commande (13', 14') écrit les données de commande dans le convertisseur parallèle/série (11') à la fois pendant l'en-tête et ultérieurement pendant les parties des trames de base qui comprennent les bits de commande.

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8. Station tête de réseau selon la revendication 7, dans laquelle l'en-tête comprend une partie de diagnostic de système, et la mémoire tampon de données de commande (13', 14') est agencée afin de sortir des impulsions de diagnostic de système dans la partie de diagnostic de système.

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9. Station tête de réseau selon l'une quelconque des revendications 6 à 8, dans laquelle la mémoire tampon de données de commande est constituée d'une paire de tampons mémoire (13', 14') reliés en parallèle entre le convertisseur parallèle/série (11') et les sorties respectives du processeur de commande (12'), de façon à ce que lorsqu'un des tampons mémoire est en train d'écrire des données dans le convertisseur parallèle/série (11'), le processeur de commande écrit des données dans l'autre des tampons mémoire.

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10. Station tête de réseau selon la revendication 9, dans laquelle les tampons mémoire (13', 14') sont des tampons mémoire de ligne vidéo.

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