CLAIMS

What is claimed is:

1. A non-planar resistive memory cell, comprising:

a first electrode disposed on opposing trench walls;

a second electrode; and

a switching layer disposed between the first and second electrodes;

wherein the second electrode is substantially between opposing portions of the switching layer.

2. The non-planar resistive memory cell of claim 1, wherein the first electrode is substantially adjacent to at least two sides of the switching layer.

3. The non-planar resistive memory cell of claim 1, wherein the first electrode is substantially adjacent to three sides of the switching layer.

4. The non-planar resistive memory cell of claim 1, wherein the first electrode is electrically connected to a voltage source and the second electrode is electrically grounded.

5. The non-planar resistive memory cell of claim 1, wherein the first electrode is electrically grounded and the second electrode is connected to a voltage source.

6. The non-planar resistive memory cell of claim 1, wherein the first and second electrodes comprise at least one of dinitride (S_2N_2), titanium nitride (TiN), tantalum nitride (TaN), copper (Cu), tungsten (W), titanium (Ti), and/or one or more noble metals.

7. The non-planar resistive memory cell of claim 1, wherein the first and second electrodes each have a thickness in the range of 5-100 nm.

8. The non-planar resistive memory cell of claim 1, wherein the switching layer comprises at least one of a metal oxide and/or a metal alloy oxide.

9. The non-planar resistive memory cell of claim 1, wherein the switching layer has a thickness in the range of 2-10 nm.

10. The non-planar resistive memory cell of claim 1, further comprising an oxygen exchange layer (OEL) disposed between the switching layer and one of the first and second electrodes.

11. The non-planar resistive memory cell of claim 10, wherein the OEL comprises at least one of hafnium (Hf), titanium (Ti), and/or tantalum (Ta).

12. The non-planar resistive memory cell of claim 10, wherein the OEL has a thickness in the range of 2-10 nm.

13. The non-planar resistive memory cell of claim 1, wherein the effective area of the cell is increased compared to a planar resistive memory cell occupying the same space.

14. The non-planar resistive memory cell of claim 1, the cell having height and width dimensions, wherein the cell height is at least five times the cell width.

15. The non-planar resistive memory cell of claim 1, wherein one of the first and second electrodes is electrically connected to a transistor in a one transistor – one resistor (1T1R) architecture.

16. The non-planar resistive memory cell of claim 1, wherein one of the first and second electrodes is electrically connected to a diode in a one diode – one resistor (1D1R) architecture.

17. Resistive random-access memory (ReRAM) comprising the non-planar resistive memory cell of any of claims 1-16.

18. A method of forming an integrated circuit, the method comprising:

etching a region in a substrate to form a first structure;

depositing a first electrode layer over the first structure to form a second structure;

depositing a sacrificial oxide layer over the second structure to form a third structure;

planarizing the third structure;

removing the sacrificial oxide layer to form a fourth structure;

depositing a switching layer material over the fourth structure to form a fifth structure;

depositing a second electrode layer over the fifth structure to form a sixth structure; and

etching the sixth structure to form a seventh structure.

19. The method of claim 18, wherein the seventh structure includes a non-planar resistive memory cell.

20. The method of any of claims 18-19, further comprising depositing an oxygen exchange layer (OEL) over the fifth structure before depositing the second electrode layer.

21. The method of any of claims 18-19, further comprising depositing an oxygen exchange layer (OEL) over the fourth structure prior to depositing the switching layer material.

22. A method of forming an integrated circuit, the method comprising:

etching a region in a substrate to form a first structure;

depositing a first electrode layer over the first structure to form a second structure;

etching the second structure to form a third structure, wherein the third structure includes first electrode spacers on side walls of the etched region in the substrate;

depositing a switching layer material over the third structure to form a fourth structure;

etching the fourth structure to form a fifth structure, wherein the fifth structure includes switching layer material substantially adjacent to the first electrode spacers;

depositing a second electrode layer over the fifth structure to form a sixth structure; and

planarizing the sixth structure to form a seventh structure.

23. The method of claim 22, wherein the seventh structure includes a non-planar resistive memory cell.

24. The method of any of claims 22-23, further comprising:

depositing an oxygen exchange layer (OEL) over the third structure, prior to depositing the switching layer material, to form a first intermediate structure; and

etching the first intermediate structure, prior to depositing the switching layer material, to form a second intermediate structure, wherein the second intermediate structure includes an OEL on the first electrode spacers.

25. The method of any of claims 22-23, further comprising:

depositing an oxygen exchange layer (OEL) over the fifth structure, prior to depositing the second electrode layer, to form a first intermediate structure; and

etching the first intermediate structure, prior to depositing the second electrode layer, to form a second intermediate structure, wherein the second intermediate structure includes an OEL on the switching layer material.

CLAIMS

What is claimed is:

1. A non-planar resistive memory cell, comprising:

a first electrode disposed on opposing trench walls;

a second electrode; and

a switching layer disposed between the first and second electrodes;

wherein the second electrode is substantially between opposing portions of the switching layer.

2. The non-planar resistive memory cell of claim 1, wherein the first electrode is substantially adjacent to at least two sides of the switching layer.

3. The non-planar resistive memory cell of claim 1 or 2, wherein the first electrode is substantially adjacent to three sides of the switching layer.

4. The non-planar resistive memory cell of any of claims 1 through 4, wherein the first electrode is electrically connected to a voltage source and the second electrode is electrically grounded.

5. The non-planar resistive memory cell of any of claims 1 through 4, wherein the first electrode is electrically grounded and the second electrode is connected to a voltage source.

6. The non-planar resistive memory cell of any of the previous claims, wherein the first and second electrodes comprise at least one of dinitride (S_2N_2), titanium nitride (TiN), tantalum nitride (TaN), copper (Cu), tungsten (W), titanium (Ti), and/or one or more noble metals.

7. The non-planar resistive memory cell of any of the previous claims, wherein the first and second electrodes each have a thickness in the range of 5-100 nm.

8. The non-planar resistive memory cell of any of the previous claims, wherein the switching layer comprises at least one of a metal oxide and/or a metal alloy oxide.

9. The non-planar resistive memory cell of any of the previous claims, wherein the switching layer has a thickness in the range of 2-10 nm.

10. The non-planar resistive memory cell of any of the previous claims, further comprising an oxygen exchange layer (OEL) disposed between the switching layer and one of the first and second electrodes.

11. The non-planar resistive memory cell of claim 10, wherein the OEL comprises at least one of hafnium (Hf), titanium (Ti), and/or tantalum (Ta).

12. The non-planar resistive memory cell of claim 10 or 11, wherein the OEL has a thickness in the range of 2-10 nm.

13. The non-planar resistive memory cell of any of the previous claims, wherein the effective area of the cell is increased compared to a planar resistive memory cell occupying the same space.

14. The non-planar resistive memory cell of any of the previous claims, the cell having height and width dimensions, wherein the cell height is at least five times the cell width.

15. The non-planar resistive memory cell of any of the previous claims, wherein one of the first and second electrodes is electrically connected to a transistor in a one transistor – one resistor (1T1R) architecture.

16. The non-planar resistive memory cell of any of claims 1 through 14, wherein one of the first and second electrodes is electrically connected to a diode in a one diode – one resistor (1D1R) architecture.

17. Resistive random-access memory (ReRAM) comprising the non-planar resistive memory cell of any of the previous claims.

18. A method of forming an integrated circuit, the method comprising:

etching a region in a substrate to form a first structure;

depositing a first electrode layer over the first structure to form a second structure;

depositing a sacrificial oxide layer over the second structure to form a third structure;

planarizing the third structure;

removing the sacrificial oxide layer to form a fourth structure;

depositing a switching layer material over the fourth structure to form a fifth structure;

depositing a second electrode layer over the fifth structure to form a sixth structure; and

etching the sixth structure to form a seventh structure.

19. The method of claim 18, wherein the seventh structure includes a non-planar resistive memory cell.

20. The method of claim 18 or 19, further comprising depositing an oxygen exchange layer (OEL) over the fifth structure before depositing the second electrode layer.

21. The method of claim 18 or 19, further comprising depositing an oxygen exchange layer (OEL) over the fourth structure prior to depositing the switching layer material.

22. A method of forming an integrated circuit, the method comprising:

etching a region in a substrate to form a first structure;

depositing a first electrode layer over the first structure to form a second structure;

etching the second structure to form a third structure, wherein the third structure includes first electrode spacers on side walls of the etched region in the substrate;

depositing a switching layer material over the third structure to form a fourth structure;

etching the fourth structure to form a fifth structure, wherein the fifth structure includes switching layer material substantially adjacent to the first electrode spacers;

depositing a second electrode layer over the fifth structure to form a sixth structure; and

planarizing the sixth structure to form a seventh structure.

23. The method of claim 22, wherein the seventh structure includes a non-planar resistive memory cell.

24. The method of claim 22 or 23, further comprising:

depositing an oxygen exchange layer (OEL) over the third structure, prior to depositing the switching layer material, to form a first intermediate structure; and

etching the first intermediate structure, prior to depositing the switching layer material, to form a second intermediate structure, wherein the second intermediate structure includes an OEL on the first electrode spacers.

25. The method of claim 22 or 23, further comprising:

depositing an oxygen exchange layer (OEL) over the fifth structure, prior to depositing the second electrode layer, to form a first intermediate structure; and

etching the first intermediate structure, prior to depositing the second electrode layer, to form a second intermediate structure, wherein the second intermediate structure includes an OEL on the switching layer material.