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ISOLATION STRUCTURE FOR A MEMORY CELL USING Al_2O_3 DIELECTRIC

FIELD OF THE INVENTION

[0001] The invention relates to an improved semiconductor structure for high density integrated circuit manufacturing and, in particular, to an improved isolation region for a memory device and a process for its formation.

BACKGROUND OF THE INVENTION

[0002] There are two major types of random-access memory cells, dynamic and static. Dynamic random-access memories (DRAMs) can be programmed to store a voltage which represents one of two binary values, but requires periodic reprogramming or "refreshing" to maintain this voltage for more than very short time periods. Static random-access memories are so named because they do not require periodic refreshing.

[0003] DRAM memory circuits are manufactured by replicating millions of identical circuit elements, known as DRAM cells, on a single semiconductor wafer. Each DRAM cell is an addressable location that can store one bit (binary digit) of data. In its most common form, a DRAM cell consists of two circuit components: a field effect transistor (FET) and a capacitor.

[0004] FIG. 1A illustrates two conventional DRAM cells 10; each cell 10 includes a capacitor 14 and an access transistor 12. For each cell 10, the capacitor 14 has two connections located on opposite sides of the capacitor 14. The first connection is to a reference voltage Vr, which is typically one half of the internal operating voltage (the voltage corresponding to a logical "1") of the memory circuit. The second capacitor connection is to the drain of the transistor 12. The gate of the transistor 12 is connected to a word line 18, and the source of the transistor is connected to a bit line 16. This connection enables the word line 18 to control access to the capacitor 14 by allowing or preventing a signal (a logic "0" or a logic "1") on the bit line 16 to be written to or read from the capacitor 14. FIG. 1C shows a cross-sectional view of the DRAM cell 10. FIG. 1B shows a portion of a DRAM memory array comprising DRAM cells 10. In FIG. 1B,

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each cell 10 sharing a given bit line 16 does not share a common wordline 18, and each cell 10 sharing a common wordline 18 does not share a common bit line 16.

[0005] DRAM manufacturing is a highly competitive business. There is continuous pressure to decrease the size of individual cells and to increase memory cell density to allow more memory to be squeezed onto a single memory chip. Cell sizes of six square feature area ($6F^2$) to four square feature area ($4F^2$) are desired (where F represents the minimum realizable photolithographic process dimension feature size). Isolation of devices on a DRAM memory thus becomes increasingly important as the size of each cell is decreased, thereby placing active areas (e.g., area 13 on FIG. 1B) of each cell in closer proximity to the active areas of other devices. Isolation is required in other integrated circuit structures as well.

[0006] Shallow trench isolation (STI) is one technique that can be used to isolate the active areas on a DRAM array or other integrated structures from one another. As shown in FIG. 1C, an isolation trench 17 formed in a substrate surface 1 may be used to isolate two adjacent DRAM memory cells, each having a capacitor 14, a transistor 12, and associated source/drain regions 19. In a typical STI isolation structure, a trench 17 is etched into the substrate and filled with one or more layers of dielectric material 15 to provide a physical and electrical barrier between adjacent active areas. Thus, an STI structure is formed by etching a trench and then filling it with a dielectric such as a chemical vapor deposited (CVD) or high density plasma (HDP) silicon oxide or silicon dioxide (SiO_2). The filled trench is then planarized by a chemical mechanical planarization (CMP) or etch-back process so that the dielectric remains only in the trench and its top surface remains level with that of the silicon substrate.

[0007] To enhance the isolation further, ions may be implanted into the silicon substrate in the area directly beneath the trench (not shown). However, there is a drawback associated with ion implantation beneath the trench; as noted, for example, in S. Nag et al., "Comparative Evaluation of Gap-Fill Dielectrics in Shallow Trench Isolation for Sub-0.25 micron Technologies," IEEE IEDM, pp. 841-844 (1996), ion implantation beneath the trench can result in high current leakage. In particular, when ions are

implanted in the substrate close to the edges of the trench, current leakage can occur at the junction between the active device regions and the trench.

[0008] Further, and referring to FIG. 1C, although deeper STI regions may provide better isolation, there is a limit to how deep the STI region can be made. If the STI region is too deep, filling the trench 17 with oxide layers 15 will result in voids 11 or cracks in the trench. Thus, there is a desire and need to isolate active areas of memory devices without relying on a deep or doped trench region.

[0009] Isolation gates have also been proposed for providing device isolation in high-density integrated circuits. These gates typically use a thick oxide layer, like silicon dioxide, but they still rely on conventional implants to provide a strong accumulation layer at the substrate surface. Thus, conventional isolation gates still facilitate the presence of gate-induced drain leakage (GIDL).

[0010] There is needed, therefore, an isolation structure which can be used in high density applications, such as DRAM memory devices. There also exists a need for a simple method of fabricating such an isolation structure.

BRIEF SUMMARY OF THE INVENTION

[0011] One exemplary embodiment of the invention provides an isolation gate formed over a substrate for biasing the substrate and providing isolation between adjacent active areas of an integrated circuit structure, for example a DRAM memory cell. An aluminum oxide (Al_2O_3) is used as a gate dielectric, rather than a conventional gate oxide layer, to create a hole-rich accumulation region under and near the trench isolation region. Another exemplary embodiment of the invention provides an aluminum oxide layer utilized as a liner in a shallow trench isolation (STI) region to increase the effectiveness of the isolation region. The embodiments may also be used together at an isolation region.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Additional advantages and features of the present invention will be apparent from the following detailed description and drawings which illustrate preferred embodiments of the invention, in which:

[0013] FIG. 1A illustrates two conventional DRAM cells in schematic form;

[0014] FIG. 1B illustrates a top-down view of a portion of a conventional DRAM array having DRAM cells constructed in accordance with FIG 1A;

[0015] FIG. 1C is a cross-sectional view of the memory cells constructed as shown in the FIG. 1A memory cell circuit;

[0016] FIG. 2A is a cross-sectional view of portions of two adjacent memory cells constructed in accordance with a first exemplary embodiment of the present invention;

[0017] FIG. 2B is a portion of a memory array having memory cells constructed in accordance with FIG. 2A;

[0018] FIG. 3 is a cross-sectional view of an exemplary memory cell of the present invention at an initial stage of fabrication;

[0019] FIG. 4 is an illustration of the memory cell of FIG. 3 at a subsequent stage of fabrication;

[0020] FIG. 5 is an illustration of the memory cell of FIG. 4 at a subsequent stage of fabrication;

[0021] FIG. 5A is an illustration of an exemplary memory cell constructed in accordance with the invention at a stage of fabrication subsequent to that of FIG. 4;

[0022] FIG. 6 is an illustration of the memory cell of FIG. 5 at a subsequent stage of fabrication;

[0023] FIG. 7 is an illustration of the memory cell of FIG. 6 at a subsequent stage of fabrication;

[0024] FIG. 8 is a is a cross-sectional view of two adjacent memory cells constructed in accordance with a second exemplary embodiment of the invention; and

[0025] FIG. 9 is a schematic diagram of a processing system employing a DRAM memory cell constructed in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0026] In the following detailed description, reference is made to various specific exemplary embodiments in which the invention may be practiced. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be employed, and that structural, logical, and electrical changes may be made.

[0027] The terms "wafer" or "substrate" used in the following description may include any semiconductor-based structure that has a semiconductor surface. Wafer and structure must be understood to include silicon, silicon-on insulator (SOI), silicon-on sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. The semiconductor need not be silicon-based. The semiconductor could be silicon-germanium, germanium, or gallium arsenide.

[0028] Referring now to the drawings, where like elements are designated by like reference numerals, a first exemplary embodiment of the invention is now described with reference to FIGS. 2A and 2B. FIG. 2A represents a cross-sectional view of portions of two exemplary DRAM memory cells 200 and FIG. 2B represents a top-down view of a partial DRAM array 201 configured with isolation gates 110 formed in accordance with a first embodiment of the present invention.

[0029] As discussed in more detail below, the isolation gate 110 of the first illustrated embodiment is preferably formed as a stacked gatestack. The isolation gate 110 has an insulating layer 114 over a conductive layer 113, which is over an aluminum oxide layer 112. Unlike the traditional grounded gate device, which contains a silicon dioxide (SiO_2) dielectric layer, the present invention proposes an aluminum oxide (Al_2O_3) gate dielectric layer 112. Al_2O_3 is a higher-k dielectric constant material (k~9.0) compared to silicon dioxide (k~3.9). Aluminum oxide creates a high negative charge density in the gate dielectric. Thus, placing aluminum oxide near the gate/p-type substrate interface, creates a hole accumulation layer near the surface of the substrate. The insulating layer 114 may be of any suitable material, such as a nitride. Suitable materials for the conductive layer 113 include, e.g., polysilicon, poly/$TiSi_2$, poly/WSi_2, poly/WN_x/W, poly/WN_x, poly/$CoSi_2$ and poly/$MoSi_2$. Oxide, nitride, or other insulating spacers 111 are provided on each side of the isolation gate 110.

[0030] Referring to FIG. 2A, the portions of the memory cells 200 are illustrated using a silicon on insulator (SOI) design with silicon layers 100, 102 and insulating layer 101, formed of, for example SiO_2. Each memory cell 200 may be formed on any semiconductor surface, however, and the invention is not limited to an SOI design, but is shown that way for exemplary purposes only.

[0031] As shown in FIG. 2A, an STI region 103 is created in substrate layer 100. A region 120 rich in positively charged holes is created along the STI sidewalls 115 and below the STI region 103 when the gate conductive layer 113 is biased by an isolation voltage V_{ISO}. This region 120 is created by providing and using the isolation gate 110, constructed in accordance with the invention, over the STI region 103.

[0032] In addition to the isolation gate 110, each memory cell 200 contains memory cell components such as transistors 104, 105 and a capacitive structure, shown schematically as a capacitors 108, 109. The transistors 104, 105 connect the memory cells 200 to an associated wordline, and the capacitors 108, 109 are electrically connected through the transistors 108, 109 to an associated bit line. The invention is, however, not limited to the embodiment of the cells 200 shown in FIG. 2A. The isolation gate 110 of

this invention may be used for providing isolation between adjacent active areas within any integrated circuit device, such as with other memory cell configurations.

[0033] In operation, the isolation gate 110 is biased by applying a grounded potential or a slight potential to the isolation gate. As illustrated in FIGS. 2A and 2B, the potential V_{ISO} represents the desired applied voltage for achieving sufficient isolation. It should be appreciated that the potential V_{ISO} may be slightly positive or negative depending on the conductivity of the gate. For an NMOS isolation gate, the aluminum oxide is biased with a slightly negative charge, thereby inducing a hole-rich accumulation region 120 under the gate 110 in the STI region 103. A potential near the range of -50 to about -400 mV, typically about -100mV, should be applied to the gatestack. If a PMOS isolation gate were utilized, a slightly positive potential would be applied to the gate in the range of about +50 to about +400 mV, typically about +100 mV. Biasing the isolation gate 110 provides electrical isolation between adjacent cells, or active areas in a cell, separated by the isolation gate 110 and corresponding isolation region 103. This electrical isolation is the result of the accumulation of electron holes along and beneath the STI region sidewalls 115, thereby preventing the flow of negative charges across this area.

[0034] In the first preferred embodiment of the invention, the aluminum oxide dielectric layer 112 produces a sufficient negative charge to keep a strong accumulation layer underneath the isolation gatestack 110 such that the gate may be maintained at ground potential. Accordingly, the isolation gate 110 of the present invention has a high threshold voltage so that when the gate is maintained at ground potential, a strong accumulation layer is created close to the surface of substrate layer 100 beneath the gate 110. For example, a typical field effect transistor in a DRAM cell, having a silicon dioxide dielectric layer, may have a threshold voltage of about 0.5 Volts. Utilizing an aluminum oxide layer 112 increases the threshold voltage of the isolation gate 110 to approximately 1.3 Volts. Although a higher threshold voltage is not always desired, in the illustrated embodiment, the higher threshold voltage is beneficial, providing an effective hole accumulation region 120.

[0035] Furthermore, the depth D of the trench isolation region 103 may be reduced when an isolation gate 110 is used in accordance with the invention. Generally, isolation trenches have a depth of about 2500Å. However, the use of an isolation gate 110 in accordance with the invention allows the use of a trench 103 having a depth D of less than about 2000Å; alternatively, in some cases, the use of an isolation trench may be altogether eliminated with sufficient device isolation being provided solely by the isolation gate formed directly on the substrate surface 100.

[0036] Referring now to FIGs. 3-7, an exemplary fabrication method performed in accordance with the first embodiment of the invention is now described. A silicon substrate layer 100 is provided. As mentioned above, the invention can be used with an SOI design, as shown in FIG. 2A; however, for the sake of simplicity, the remaining figures and description will describe a silicon substrate semiconductor design.

[0037] An initial stage of fabrication is now described with reference to FIG. 3. It is desirable that the STI regions 103 are formed in the substrate 100 prior to formation of the transistors 104, 105; and accordingly, it is desired that the isolation gate 110 is formed subsequent to the formation of the underlying source/drain regions 106, 107 that are located adjacent the isolation trench 103. The isolation trench 103 can be formed by any suitable method, such as by etching a trench by a dry anisotropic or other etching process. After etching, the trench is then filled with a dielectric, for example, by a chemical vapor deposited (CVD) or high density plasma (HDP) deposition of silicon oxide or silicon dioxide. Next, the filled trench 103 is planarized by a chemical mechanical polishing (CMP) or etch-back process so that the dielectric remains only in the trench and its top surface remains level with that of the silicon substrate 100. Source drain regions 106, 107 may be implanted regions using conventional implantation processes. Next, a very thin gate oxide layer 130 is grown everywhere over the surface of the substrate 100 to act as a buffer layer.

[0038] FIG. 4 illustrates a subsequent step in fabricating the memory cell 200. A layer of aluminum oxide 112 is deposited to a desired thickness over the buffer layer 130. The deposition of the aluminum oxide layer 112 can be performed by any suitable method

including, but not limited to, chemical vapor deposition (CVD), plasma vapor deposition, or atomic layer deposition. Because aluminum oxide is a higher-k material than conventional gate oxides, a thicker film layer may be utilized to provide the same effective oxide thickness as in the conventional DRAM cell. This is advantageous since depositing a thicker film allows more process control by reducing variation in film thickness across a large wafer. The thickness of the aluminum oxide film is generally about 50 to about 150 Angstroms, preferably 100-115 Angstroms.

[0039] FIG. 5 shows a conductive layer 113 that is selectively deposited over the aluminum oxide layer 112. After patterning, the conductive layer 113 is located over the isolation trench 103. The conductive layer 113 may be any type of conductor used in conventional gate structures, and is preferably formed of the same material as the other transistor gates 104, 105 of the memory cell 200.

[0040] It should be understood that alternatively, an additional gate dielectric 117 may be deposited over the aluminum oxide layer 112 before the conductive layer 113 is deposited, as shown in Fig. 5A. This additional dielectric layer 117 may be any suitable gate dielectric including, but not limited to, a silicon dioxide layer. Like the conductive layer 113, this additional dielectric layer 117 is patterned for deposit only over the area where the gate 110 is to be formed. This step could be done simultaneously with the deposition of the first dielectric layer for the gates of other transistors 104, 105 on the array. If so, the dielectric material 117 would also be selectively deposited where the gatestacks for the transistors 104, 105 are to be formed.

[0041] FIG. 6 shows the next step in forming the isolation gate 110, with reference back to the memory cell 200 after completion of the steps shown in FIG. 5. A dielectric layer 114 is selectively deposited over the conductive layer 113. The dielectric layer 114 can be any suitable gate insulating layer compatible with the other layers of the gatestack, and may be for example, a nitride or an oxide. The dielectric layer is pattern-deposited over the electrode layer 113.

[0042] FIG. 7 shows that the aluminum oxide 112 is etched with any suitable etchant, by using a mask over the gatestack 110 to etch the aluminum oxide 112 everywhere except under the conductive and dielectric layers, 113 and 114, respectively. This completes the isolation gate stack 110. Insulating sidewalls 111 may be formed on either or each side of the isolation gate stack 110. Sidewalls 111 may be formed of oxide, nitride, or any other suitable insulating material.

[0043] Conventional processing steps may then be carried out to complete formation of the memory cells. For instance, with reference to the exemplary cells 200 of FIG. 2A, transistors 104, 105 can be formed using any suitable method and using conventional gate oxide layer, e.g., silicon dioxide, in the gatestacks. The transistor gatestacks are located above and electrically connected to the source drain regions 106, 107. To the extent feasible, the conductive and second dielectric layers of the gatestacks of the transistors 104, 105 may be formed at the same time as the formation of the isolation gate 110. If so, this requires that the aluminum oxide is selectively etched, as discussed with reference to FIG. 7, as soon as it is deposited. Then, conductive layer 113 and dielectric layer 114, can be selectively deposited for each transistor 104, 105 gatestack and also as part of the isolation gatestack. Capacitors 108, 109 are formed using any suitable method and are electrically connected to an associated bit line on the memory array 201 (FIG. 2B) through the transistors 104, 105.

[0044] The isolation gate 110 as just described may be implemented in memory cell arrays using a wide variety of transistor and capacitor configurations. In addition, the invention may be utilized to provide isolation for very high density memory cells, such as in $6F^2$ or $4F^2$ cells as discussed above. This invention is in no way limited to a specific design of the memory cell.

[0045] FIG. 8 illustrates a second embodiment of the invention. Here, the active regions of two memory cells 300 are separated by a trench isolation region 303 that utilizes aluminum oxide as a thin lining 304 within an isolation trench. The trench may be formed by anisotropic etching, or any other suitable method, to a depth of about 1,000 to about 4,000 Angstroms. The aluminum oxide layer 304 is deposited to line the trench. The

aluminum oxide may be deposited over the entire surface of the substrate 301 to insure that the side walls and bottom of the trench are coated. Chemical vapor disposition, plasma vapor deposition, or any other suitable technique may be used to deposit the aluminum oxide layer 304 to a thickness of about 30 to about 500 Angstroms, preferably about 50 to 100 Angstroms. Alternatively, a suitable high-k dielectric material, such as aluminum nitride or other silicon-rich aluminum oxides, may be used instead of the aluminum oxide.

[0046] Subsequently, a dielectric material 305 is deposited in the trench region 303. Any suitable dielectric material may be used; for example, the trench can be filled with silicon dioxide, silicon nitride, oxide-nitride, or oxide-nitride-oxide. The entire substrate 301 is planarized, removing excess dielectric material 305 as well as any aluminum oxide 304, from the surface of the substrate 301. Conventional processing steps are then used to complete formation of the memory cell, including formation of capacitors 308, 309 and transistors 310, 311 and other memory cell elements as desired.

[0047] Similar to the memory cells 200 discussed above with reference to FIG. 2A, the memory cells 300 are isolated by a highly effective isolation region 303. Utilizing aluminum oxide as a trench liner 304 will minimize the current leakage across the region 303, thereby better isolating active areas of the memory cell 300.

[0048] Like the grounded gate 110 (shown in FIG. 2A), the trench isolation region 303 of the second embodiment is in no way limited to the design or configurations of the memory cell 300. The trench isolation region 303 constructed in accordance with the present invention may be utilized to isolate active areas between any adjacent memory cells, without being limited to a specific configuration.

[0049] It should be appreciated that the isolation region provided by the first and second embodiments of the invention may also be used in conjunction with eachother and with other isolation structures and techniques. For example, the isolation gatestack 110 may be constructed, as described above, over an isolation trench region 303 having an

aluminum oxide liner. The invention can also be combined with other known isolation techniques for memory cells that are not described in detail herein.

[0050] FIG. 9 illustrates an exemplary processing system 900 that utilizes a memory device 840 containing an array 201 of DRAM memory cells 200 or 300 isolated as described above. The processing system 900 includes one or more processors 901 coupled to a local bus 904. A memory controller 902 and a primary bus bridge 903 are also coupled the local bus 904. The processing system 900 may include multiple memory controllers 902 and/or multiple primary bus bridges 903. The memory controller 902 and the primary bus bridge 903 may be integrated as a single device 906.

[0051] The memory controller 902 is also coupled to one or more memory buses 907. Each memory bus accepts memory components 908, which include at least one memory device 840 containing the improved isolation region in accordance with the invention. Alternatively, in a simplified system, the memory controller 902 may be omitted and the memory components directly coupled to one or more processors 901. The memory components 908 may be a memory card or a memory module. The memory components 908 may include one or more additional devices 909. For example, the additional device 909 might be a configuration memory. The memory controller 902 may also be coupled to a cache memory 905. The cache memory 905 may be the only cache memory in the processing system. Alternatively, other devices, for example, processors 901 may also include cache memories, which may form a cache hierarchy with cache memory 905. If the processing system 900 include peripherals or controllers which are bus masters or which support direct memory access (DMA), the memory controller 902 may implement a cache coherency protocol. If the memory controller 902 is coupled to a plurality of memory buses 907, each memory bus 907 may be operated in parallel, or different address ranges may be mapped to different memory buses 907.

[0052] The primary bus bridge 903 is coupled to at least one peripheral bus 910. Various devices, such as peripherals or additional bus bridges may be coupled to the peripheral bus 910. These devices may include a storage controller 911, an miscellaneous I/O device 914, a secondary bus bridge 915, a multimedia processor 918, and an legacy

device interface 920. The primary bus bridge 903 may also coupled to one or more special purpose high speed ports 922. In a personal computer, for example, the special purpose port might be the Accelerated Graphics Port (AGP), used to couple a high performance video card to the processing system 900.

[0053] The storage controller 911 couples one or more storage devices 913, via a storage bus 912, to the peripheral bus 910. For example, the storage controller 911 may be a SCSI controller and storage devices 913 may be SCSI discs. The I/O device 914 may be any sort of peripheral. For example, the I/O device 914 may be an local area network interface, such as an Ethernet card. The secondary bus bridge may be used to interface additional devices via another bus to the processing system. For example, the secondary bus bridge may be an universal serial port (USB) controller used to couple USB devices 917 via to the processing system 900. The multimedia processor 918 may be a sound card, a video capture card, or any other type of media interface, which may also be coupled to one additional devices such as speakers 919. The legacy device interface 920 is used to couple legacy devices, for example, older styled keyboards and mice, to the processing system 900.

[0054] The processing system 900 illustrated in FIG. 9 is only an exemplary processing system with which the invention may be used. While FIG. 9 illustrates a processing architecture especially suitable for a general purpose computer, such as a personal computer or a workstation, it should be recognized that well known modifications can be made to configure the processing system 900 to become more suitable for use in a variety of applications. For example, many electronic devices which require processing may be implemented using a simpler architecture which relies on a CPU 901 coupled to memory components 908 and/or memory elements 200. The modifications may include, for example, elimination of unnecessary components, addition of specialized devices or circuits, and/or integration of a plurality of devices.

[0055] The description and drawings presented above illustrate only a few of the many embodiments which achieve the features and advantages of the present invention. Modification and substitutions to specific process conditions and structures can be made

without departing from the spirit and scope of the present invention. Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.

CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of forming a memory array, said method comprising:

forming a plurality of memory cells over a substrate, each cell comprising at least one active area; and

forming an isolation region adjacent to and between said active areas of two adjacent memory cells, said isolation region comprising a layer of aluminum oxide.

2. The method of claim 1, wherein the step of forming an isolation region comprises forming a trench in said substrate and lining said trench with said layer of aluminum oxide.

3. The method of claim 1, wherein the step of forming an isolation region comprises forming a trench in said substrate and forming a gate above the trench, said gate comprising said layer of aluminum oxide.

4. A method of forming a memory cell comprising:

forming a plurality of active areas in a substrate;

forming a trench region in said substrate and located between adjacent active areas;

filling said trench region with an insulating material; and

providing a layer of aluminum oxide over said trench region to form an isolation region.

5. The method of claim 4, wherein the step of providing a layer of aluminum oxide comprises depositing an aluminum oxide film over the surface of said substrate.

6. The method of claim 5, wherein said aluminum oxide film has a thickness of about 80 to about 120 Angstroms.

7. The method of claim 5, further comprising the step of etching said aluminum oxide film everywhere except for a selected area over said trench region.

8. The method of claim 7, further comprising the step of depositing a conductive layer over said aluminum oxide film.

9. The method of claim 8, further comprising the step of depositing an insulating layer comprising a nitride over said conductive layer.

10. The method of claim 5, wherein the step of depositing an aluminum oxide film comprises:

depositing a thin buffer layer over a top surface of said substrate; and

depositing said aluminum oxide film over said thin buffer layer.

11. The method of claim 10, wherein the step of depositing an aluminum oxide film comprises performing a chemical vapor deposition process (CVD) to form said aluminum oxide film.

12. The method of claim 11, further comprising the step of providing a conductive layer over said aluminum oxide film.

13. The method of claim 12, further comprising the step of depositing an insulating layer over said conductive layer to

form an isolation gatestack, wherein said insulating layer comprises one of a nitride and aluminum oxide.

14. The method of claim 13, further comprising the step of etching said aluminum oxide film everywhere except under the area where said isolation gatestack is formed.

15. The method of claim 13, wherein said conductive layer comprises one of polysilicon, poly/$TiSi_2$, poly/WSi_2, poly/WN_x/W, poly/WN_x, poly/$CoSi_2$ and poly/$MoSi_2$.

16. A method of isolating active areas of a memory cell array comprising:

providing a memory cell array, each memory cell of said array comprising at least one active area and an isolation gate comprising a layer of aluminum oxide, said gate adjacent said at least one active area;

connecting said isolation gate to a terminal for receiving a voltage potential; and

applying the potential to said isolation gate through said terminal.

17. The method of claim 16, wherein said applied potential is negative.

18. The method of claim 17, wherein said applied potential is in the range of about -50 to about -400 mV.

19. The method of claim 16, wherein said applied potential drives said gate to ground.

20. A method of forming an isolation region between active areas on a memory cell array, said method comprising:

providing a memory cell array having a plurality of active areas formed on a substrate;

etching a shallow trench in the substrate between two adjacent active areas of said array; and

lining said trench with an aluminum oxide layer.

21. The method of claim 20, wherein said trench is etched to a depth of about 1000 to about 4000 Angstroms.

22. The method of claim 20, wherein the step of lining said trench comprises depositing aluminum oxide over the sidewalls and bottom of the trench and over the substrate surface.

23. The method of claim 22, wherein the step of lining said trench comprises a masking step to selectively deposit said aluminum oxide layer.

24. The method of claim 22, further comprising the step of planarizing the substrate surface to remove excess aluminum oxide from the substrate surface while leaving the aluminum oxide in said trench.

25. The method of claim 22, wherein said aluminum oxide layer has a thickness of about 30 to about 500 Angstroms.

26. The method of claim 25, wherein said aluminum oxide layer has a thickness of about 50 to about 100 Angstroms.

27. The method of claim 22, further comprising the step of filling said lined trench with a dielectric material.

28. A memory cell array comprising:

a plurality of memory cells formed on a substrate and being arranged into rows and columns;

a plurality of wordlines electrically connected to the rows;

a plurality of bit lines electrically connected to the columns;

wherein each memory cell comprises:

at least one access transistor for connecting said cell to a respective wordline;

at least one capacitor electrically connected though said at least one access transistor to a respective bit line; and

an isolation region located adjacent said at least one capacitor, said isolation region comprising a layer of aluminum oxide.

29. The memory cell array of claim 28, wherein said isolation region is a trench in said substrate and is capable of forming a hole accumulation region surrounding said trench.

30. The memory cell array of claim 29, wherein said aluminum layer comprises a liner of said trench formed in said substrate.

31. The memory cell array of claim 28, wherein said isolation region comprises:

a trench formed in said substrate; and

a gatestack located over said trench, wherein said gatestack comprises said layer of aluminum oxide.

32. The memory cell array of cell 31 wherein said isolation region is capable of forming a hole accumulation region surrounding said trench.

33. The memory cell array of claim 28, wherein said array is a high density dynamic access memory (DRAM) array.

34. A memory cell comprising:

a substrate;

a capacitive structure formed over said substrate;

an access transistor formed at least partially on said substrate and electrically connected to said capacitive structure; and

an isolation gate comprising a layer of aluminum oxide formed over a top surface of said substrate and adjacent at least one active area of said substrate.

35. The memory cell of claim 34, wherein the cell is a DRAM cell.

36. The memory cell of claim 35, wherein the cell is a $6F^2$ DRAM cell.

37. The memory cell of claim 34, wherein said isolation gate is located over a trench region formed in said substrate.

38. The memory cell of claim 34, wherein said isolation gate further comprises a conductive layer deposited over said aluminum oxide layer.

39. A memory cell comprising:

a substrate;

an active area in said substrate;

a capacitive structure formed over said substrate and electrically connected to the active area;

an access transistor electrically connected to said capacitive structure; and

a trench isolation region formed in said substrate adjacent the active area, wherein said trench region is lined with a thin layer of aluminum oxide.

40. The memory cell of claim 39, wherein said access transistor is an NMOS transistor.

41. The memory cell of claim 39, wherein the trench isolation region further comprises a dielectric insulating material.

42. The memory cell of claim 39, wherein said aluminum oxide layer is in contact with the sidewalls of the isolation trench.

43. The memory cell of claim 39, wherein said trench isolation region is located adjacent said capacitive structure.

44. An integrated circuit memory cell comprising:

a substrate;

a capacitor formed over an active area in said substrate;

an access transistor electrically connected to said capacitor; and

an isolation region comprising a layer of aluminum oxide and a trench region, said isolation region formed adjacent the active area.

45. The integrated circuit memory cell of claim 44, wherein said isolation region further comprises a gatestack comprising said aluminum oxide layer.

46. The integrated circuit memory cell of claim 45, wherein said gatestack is adapted for connection to a terminal for receiving a voltage potential.

47. The integrated circuit memory cell of claim 46, wherein said gatestack is formed above said trench region.

48. The integrated circuit memory cell of claim 47, further comprising source/drain regions adjacent said shallow trench isolation region.

49. The integrated circuit memory cell of claim 48, wherein said source/drain regions comprise slightly negatively- doped regions.

50. The integrated circuit memory cell of claim 44, wherein said aluminum oxide layer is located in said trench region.

51. The integrated circuit memory cell of claim 50, wherein said aluminum oxide layer lines the sidewalls and bottom of said trench.

52. A memory cell array comprising:

a plurality of memory cells formed in a substrate, wherein a plurality of the cells of the array comprise:

at least one active area in the substrate;

an access transistor formed over the substrate surface and electrically connected to a capacitive structure; and

an isolation gate for reducing charge leakage in the substrate between active areas in the array, wherein said gate comprises a layer of aluminum oxide.

53. The array of claim 52, wherein said memory cells are dynamic random access (DRAM) memory cells.

54. The array of claim 53, wherein said memory cells are $6F^2$ DRAM cells.

55. The DRAM array of claim 53, wherein said isolation gate is located over an isolation trench formed in said substrate.

56. A computer system, comprising:

a processor; and

a dynamic random access memory (DRAM) array fabricated on a semiconductor chip communicating with the processor, said DRAM array comprising:

a plurality of DRAM memory cells, each cell having at least one active area; and

isolation devices, for isolating said active areas and being formed in said chip, wherein said isolation devices comprise a gatestack having an aluminum oxide layer.

57. A computer system, comprising:

a processor; and

a dynamic random access memory (DRAM) array fabricated in a semiconductor substrate communicating with the processor and comprising:

a plurality of DRAM memory cells, each cell having at least one active area; and

isolation regions, for isolating said at least one active area from other areas of the memory cell, wherein said isolation regions each comprise a trench region etched in said substrate and lined with an aluminum oxide layer.