

Phase Change Material Memory Device

Background

This invention relates generally to electronic memories and particularly to electronic memories that use phase change material.

5 Phase change materials may exhibit at least two different states. The states may be called the amorphous and crystalline states. Transitions between these states may be selectively initiated. The states may be distinguished because the amorphous state generally exhibits higher resistivity than the crystalline state. The amorphous state involves a more disordered atomic structure. Generally any phase change material may be utilized. In some
10 embodiments, however, thin-film chalcogenide alloy materials may be particularly suitable.

 The phase change may be induced reversibly. Therefore, the memory may change from the amorphous to the crystalline state and may revert back to the amorphous state thereafter, or vice versa, in response to temperature changes. In effect, each memory cell may be thought of as a programmable resistor, which reversibly changes between higher and
15 lower resistance states. The phase change may be induced by resistive heating.

 In some embodiments, the cell may have a large number of states. That is, because each state may be distinguished by its resistance, a number of resistance determined states may be possible, allowing the storage of multiple bits of data in a single cell.

 A variety of phase change alloys are known. Generally, chalcogenide alloys contain
20 one or more elements from Column VI of the periodic table. One particularly suitable group of alloys is the GeSbTe alloys.

 A phase change material may be formed within a passage or pore through an insulator. The phase change material may be coupled to upper and lower electrodes on either end of the pore.

25 One problem that arises is that the adherence between the insulator and the phase change material may be poor. One solution to this problem is to provide an interfacial layer that promotes adhesion between the insulator and the phase change material. Generally, suitable interfacial layers are conductors such as titanium.

 In particular, because of the use of extended lengths of phase change material, the
30 possibility of separation arises. The use of column stripes of phase change material may require adhesion along long stripes despite the thermal expansion and contraction from subsequent processing steps. There is also accumulative stress along the column line from

- 2 -

the phase change material stack itself and from subsequent thin-film depositions required as part of integration into an integrated circuit process flow.

Alternatively, a glue layer may be positioned between the insulator and the phase change material. However, the glue layer may degrade the phase change material or add
5 processing cost.

Another issue with existing phase change memories is upwardly directed heat loss through the cell. The more the heat loss, the greater the programming current that is required since heat is utilized to induce the programming phase change.

Still another problem is the incorporation of species from the upper electrode into the
10 phase change material. Species incorporation can have detrimental effects on programming properties of the phase change material.

Yet another issue with existing phase change material memories is the need for dry etching of the phase change material. The dry etch of a phase change material stack is a complicated process. Issues of undercut and re-entrant profiles may be encountered.

15 Thus, there is a need for better designs for phase change memories that may be manufactured using more advantageous techniques.

Brief Description of the Drawings

Figure 1 is an enlarged, cross-sectional view in accordance with one embodiment of
20 the present invention;

Figure 2 is an enlarged, cross-sectional view of the device shown in Figure 1 taken transversely to the view shown in Figure 1;

Figure 3 is a top plan view of the embodiment shown in Figures 1 and 2;

Figure 4 is an enlarged cross-sectional view of the initial processing of the structure of
25 Figure 1 in accordance with one embodiment of the present invention;

Figure 5 shows subsequent processing on the structure shown in Figure 4 in accordance with one embodiment of the present invention;

Figure 6 shows subsequent processing of the structure shown in Figure 5 in accordance with one embodiment of the present invention; and

30 Figure 7 shows subsequent processing of the embodiment shown in Figure 6 in accordance with one embodiment of the present invention.

- 3 -

Detailed Description

Referring to Figure 1, a phase change memory cell 10 may be formed on a substrate 12 that in one embodiment may be a silicon substrate. A pair of lower electrodes 14 may be formed over the substrate 12. The electrodes 14 may be separated by an insulator 16. A pore may be formed above the lower electrode 14 between the lower electrode 14 and the top electrode 28. The pore may include a tapered, cup-shaped phase change material 18 covered by a similarly shaped barrier layer 20. A fill insulator 22 may fill the central portion of the barrier 20 and the phase change material 18. An etch stop layer 24 underlies a barrier layer 26 that in turn underlies the top electrode 28.

Referring to Figure 2, the top electrode 28 extends along two adjacent pores. The pores may be separated by an insulator 16. Cells defined by the pores may be distributed in large numbers across the substrate 12 in some embodiments. As viewed from above in Figure 3, each electrode 28 covers a plurality of pores including the elements 14, 18, 20 and 22, separated by insulator 16 covered by an etch stop layer 24.

A technique for forming the memory cells 10, according to one embodiment, may involve initially forming the lower electrodes 14 on a substrate 12 using conventional patterning and deposition techniques, as shown in Figure 4. Any conventional technique may be utilized to form the electrodes 14. The electrodes 14 may be formed of a variety of conductors including cobalt silicide.

The insulator 16 may then be deposited over the patterned lower electrodes 14. In one embodiment, the insulator 16 is an electrical and thermal insulator. One suitable material is silicon dioxide that may be from about 50 to 1500 Angstroms thick in one embodiment. Next a planarization such as, for example, a chemical mechanical planarization (CMP) is performed to achieve global and local planarity. This may be followed by the deposition, if desired, of a CMP etch stop layer 24. The layer 24 may be silicon nitride or polysilicon having a thickness from 10 to 1000 Angstroms in one embodiment.

Referring next to Figure 5, the pore openings 32, defined through the etch stop layer 24, receive a side wall spacer 30. The side wall spacer 30 may be formed using standard techniques of depositing an insulating layer and selectively anisotropically dry etching that layer from the lower electrode 14 and the etch stop layer 24. An insulating spacer 30 may be made of silicon dioxide or nitride such as Si_3N_4 . The thickness of the insulating spacer 30 may be in the range of 50 to 2000 Angstroms in one embodiment.

- 4 -

Turning next to Figure 6, deposited in a sequential fashion over the structure shown in Figure 5 may be the phase change layer 18, barrier layer 20, and fill insulator 22, in one embodiment. The phase change material 18 may be a chalcogenide-based material such as $\text{Ge}_2\text{Sb}_2\text{Te}_5$ with a thickness of 50 to 1000 Angstroms in one embodiment. The barrier material 20 may be, for example, titanium, titanium nitride or titanium-tungsten, for example, with a thickness in the range of 10 to 500 Angstroms. The fill insulator 22 may be any insulator with low thermal and electrical conductivity. Examples of suitable fill insulator 22 materials include silicon dioxide or silicon nitride, such as Si_3N_4 with a thickness of about 500 to 10,000 Angstroms, for example.

Turning finally to Figure 7, CMP removes the fill insulator 22, barrier layer 20, and phase change material 18 in all regions above the etch stop layer 24. CMP thereby defines the structure of the phase change material 18 while eliminating the need for a dry etch in one embodiment. As mentioned earlier, the use of the dry etch may complicate the process flow and raise issues of undercut and re-entrant profiles. Moreover, because the phase change material 18 is defined within an encapsulated, singulated region, the problem of adhesion between the phase change material 18 and the surrounding materials may be substantially reduced or even eliminated, even after exposure to ensuing thermal stresses.

The imposition of the insulator 22 over the phase change material 18 reduces upward thermal losses. Thermal losses may result in the need for greater programming currents to obtain the same programming effect.

As shown in Figure 1, the structure of Figure 7 may be covered with a barrier layer 26 and a top electrode 28. In one embodiment, the barrier layer 26 may be titanium, titanium nitride, or titanium-tungsten at a thickness in the range of 10 to 500 Angstroms. The top electrode 28 may be aluminum copper alloy in one embodiment with a thickness in the range of 200 to 20,000 Angstroms. The use of a barrier layer 26 may reduce the incorporation of species from the top electrode 28 into the phase change material 18 in some embodiments. The top electrode 28 and barrier layer 26 may be patterned using standard photolithographic and dry etching techniques to achieve the structures shown in Figure 1, 2, and 3.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

- 5 -

What is claimed is:

1. A method comprising:
defining a singulated opening in an insulating layer,
forming a cup-shaped chalcogenide material entirely in said opening; and
forming a thermally insulating material in said cup-shaped chalcogenide material.
2. The method of claim 1 including forming an electrode and a barrier layer, said electrode coupled to said chalcogenide material through said barrier layer.
3. The method of claim 1 including forming an electrode electrically coupled to said chalcogenide material, and isolating species in said electrode from said chalcogenide material using a barrier layer.
4. The method of claim 1 including insulating said chalcogenide material to reduce upwardly directed heat loss.
5. The method of claim 1 including defining said chalcogenide material using a planarization process.
6. The method of claim 5 including defining said chalcogenide material using a chemical mechanical planarization technique.
7. The method of claim 1 including defining a side wall spacer in said singulated opening.
8. The method of claim 7 including defining an electrode in said opening.
9. The method of claim 8 including using said side wall spacer to define the cup-shape of said chalcogenide material.

- 6 -

10. A method comprising:
defining a phase change material;
forming an electrode over said phase change material; and
depositing a titanium barrier layer in contact with said phase change material and electrode such that without said titanium barrier layer said electrode contact said phase change material.
11. The method of claim 10 including forming said barrier layer of a thickness of 500 Angstroms or less.
12. The method of claim 11 including forming said barrier layer of titanium nitride.
13. A method comprising:
defining an opening in a structure;
forming a layer of chalcogenide material into said opening and over said structure; and
planarizing said chalcogenide material.
14. The method of claim 13 including chemical mechanical planarizing said chalcogenide material.
15. The method of claim 13 including forming a side wall spacer in said opening and then depositing said chalcogenide material.
16. The method of claim 13 including forming a cup-shaped chalcogenide material.
17. The method of claim 16 including filling said cup-shaped chalcogenide material with an insulator.

- 7 -

18. A memory comprising:
a support structure;
an insulator over said support structure, said insulator having an opening defined in said insulator; and
a cup-shaped phase change material in said opening, said cup-shaped phase change material arranged substantially entirely within said opening in said insulator.

19. The memory of claim 18 including an insulator in said cup-shaped phase change material.

20. The memory of claim 18 wherein said phase change material is encapsulated.

21. The memory of claim 18 wherein said phase change material is singulated.

22. The memory of claim 18 wherein said cup-shaped phase change material includes a cup-shaped portion, said cup-shaped portion being filled with an insulator.

23. The memory of claim 18 including a side wall spacer in said opening.

24. A memory comprising:
a support structure;
an insulator over said support structure, said insulator having an opening defined in said insulator; and
a cup-shaped phase change material in said opening, said phase change material including an upper surface and said insulator including an upper surface, said upper surfaces of said insulator and said phase change material being substantially coplanar.

- 8 -

25. The memory of claim 24 wherein said phase change material includes a cup-shaped portion and a filler insulator formed in said cup-shaped portion.

26. The memory of claim 24 wherein said filler insulator includes an upper surface, the upper surface of said insulator being substantially coplanar with the upper surfaces of said filler insulator and said phase change material.

27. The memory of claim 24 wherein said phase change material is singulated.

28. The memory of claim 24 wherein said phase change material is encapsulated.

29. The memory of claim 24 including a side wall spacer in said opening.