

PATENT SPECIFICATION

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(54) CURRENT SOURCE

(71) We, GENERAL ELECTRIC COMPANY, a corporation organised and existing under the laws of the State of New York, United States of America, of 1 River Road, Schenectady 12305, State of New York, United States of America do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a current source which is an improvement in or modification of the current source claimed in our co-pending Patent Application No. 41909/77 (Serial No. 1,503,173).

The present invention is a current source comprising an output transistor of a first conductivity type for providing at its collector a d.c. output current, a direct coupled amplifier controlling said output transistor, and first and second inputs to said amplifier, the arrangement being such that a d.c. signal applied to the second input determines the static d.c. level of the output current and the dynamic level of the output current is determined by a signal supplied to the first input, the source further including a power supply line to which is connected, via a first resistance, the emitter of the output transistor, the current source further comprising, connected between the base of the output transistor of the current source and the power supply line a series combination of (1) a semiconductor diode device which is poled to conduct current in the same direction as the direction of emitter current flow of the current source's output transistor, and of (2) a second resistance, said series combination, in operational use, serving to conduct a current with which is combined the base current of the output transistor, that base current being amplified by the output transistor, the magnitude of the latter combined current and hence of the output transistor's base current being

determinable by the potential established at the output transistors base, said direct coupled amplifier including a first and a second additional transistor, each of a second conductivity type opposite to the first conductivity type, the collectors of the first and second additional transistors being connected together and to the base of the output transistor, the base of the first additional transistor constituting the first input of the current source, and the emitter of the second additional transistor constituting said second input being connected to a resistive connection—itsself comprising a resistance having an end connected to the latter emitter,—the latter resistive connection being alternatively connectible in operational use of the current source, either to a primary reference point or line so as to render said second additional transistor conductive and thereby determine one static d.c. level of the current source's output current, or to a line or point which in operational use is at a steady d.c. potential sufficiently high to cut off said second additional transistor, and thereby determine another static d.c. level of the current source's output current, and the base of the second additional transistor being connected to a secondary reference point or line.

An embodiment of the present invention will now be described, by way of example, with reference to the accompanying drawings in which:—

Figure 1 is a drawing partly in block and partly in electrical circuit diagram form of a superheterodyne receiver incorporating a current source in accordance with the invention and an AM-FM detector.

Figure 2 is an equivalent circuit representation of the AM detection portion of the radio receiver illustrated in Figure 1;

Figure 3 is an equivalent circuit representation of the FM detection portion of the receiver illustrated in Figure 1; and Figure 4 is a graph illustrating both the

amplitude response and the phase response as a function of frequency of the phase shift network used in FM detection.

A radio receiver embodying the invention is shown in the combined block and electrical circuit diagram of Figure 1. The radio receiver of Figure 1 is a superheterodyne receiver intended for AM-FM operation. The receiver has an AM-FM converter (block 11) an IF amplifier functioning on two IF frequencies, all but one stage of which are included in block 12, and at least one current source. The last stage (Q11, Q12) of IF amplification is included in the circuit diagram portion of Figure 1 which also includes the input filters (18, 19) for the AM-FM detector, the AM-FM detector itself, and the initial audio preamplification. The receiver is completed with an output

audio amplifier (block 13), and a capacitively coupled loudspeaker (14). Of particular interest is the AM-FM detector the last IF amplification stage (Q11, Q12) as regards both the emitters' d.c. stabilization circuit or current source 123, and the manner of loading the FM-filter 18 and the AM-filter 19, and the AFC-AGC amplifier or current source 129.

Reference is made to our copending applications No. 2681/75 (Serial No. 1,503,171), No. 35886/77 (Serial No. 1,503,172), and No. 41909/77 (Serial No. 1,503,173), which collectively relate to an AM-FM radio receiver similar to that disclosed herein and are hereinafter collectively referred to as McFadyen et al I, or simply McFadyen I; the following tabulation indicated the correspondence as between Figure 1 hereof, and McFadyen I.

Figure 1 hereof AM-FM Converter 11

IF amplifier 12 including final stage transistors Q11 and Q12, and their associated circuitry, including tuned circuits 19 and 18, and current source 123;

AFC-AGC current source 129 including (1) output PNP-transistor Q15 which delivers output AFC-AGC current or voltage via "primary bus" 118 to the IF amplifier 12 and to AM-FM converter 11; (2) "reference" for current source (diode D6 and resistance 48); (3) amplifier NPN-transistors Q16 and Q17, the former receiving "dynamic" AFC or AGC d.c. signal on line 165, and the latter receiving static d.c. input signal

FM-AM detector of Figure 1

Concerning the sense of the AM-AGC signal, the indicated "dot-convention" for the AM-detector tuned circuit or filter 19 assure the following sense, which is required for AGC-purposes; see also Figure 2. Increased amplitude of the incoming AM-IF carrier results in more positive dynamic d.c. AGC signal at the outputs of NPN-transistors Q1 and Q2, and Q3, but more negative dynamic d.c. AGC signal at the output (collector) of PNP transistor Q5 and hence on line 165 and the base of the AFC-AGC current source input NPN-transistor Q16. Q16 inverts the sense, but then the PNP output transistor Q15 re-inverts the sense, so that the primary bus 118 delivers more negative (less positive)

McFadyen I

FM and AM local oscillators and mixers described therein

IF amplifier 10 including final stage transistors Q7 and Q8, and their associated circuitry, including tuned circuit 25, and current source 24 also "secondary AGC bus 19" for the IF amplifier.

AFC-AGC current source 29 including (1) output PNP-transistor Q27 which delivers output AFC-AGC current or voltage via "primary bus" 18 to the IF amplifier 10 and to the AM-FM converter; (2) "reference" for current source (diode-connected transistor Q23 and resistance 51); (3) amplifier NPN-transistors Q25, which receives "dynamic" AFC or AGC d.c. signal on line 65, Q24, and Q26, with Q26 receiving static d.c. input signal

FM-AM detector 26

dynamic d.c. AGC signal current and voltage.

The sense of the dynamic AFC d.c. signal is as follows; refer also to Figure 3. When the frequency of the incoming FM-IF modulation carrier is too low in the output of the selection circuit (emitters of Q1 and Q2), i.e. in the waveform 36 in Figure 3, the $90^\circ \pm 25^\circ$ spacings between zero-crossings are widened, and this gives rise to two d.c. effects: (1) the composite static plus dynamic level 236 is decreased; this is of no consequence, because as indicated above and further explained hereinafter, the limiter or zero-crossing detector (Q8, Q9) is insensitive to the shift in level 236; (2) in the output of the zero-crossing detector,

(collector of Q9), i.e. in the waveform 37, the narrow pulses are widened and in consequence the average d.c. level 137, which is the dynamic AFC d.c. voltage, is reduced. The PNP transistor Q10 at its collector, and on line 165 and the base of Q16, inverts the sense of the AFC signal to more positive AFC voltage; Q16 further inverts to more negative AFC voltage, but the current source (129) PNP output transistor Q15 at its collector (and primary bus 118) reinverts to a more positive current and voltage delivered to the blocks 12 and 11. In either AM-mode or FM-mode, carried along with the AGC or AFC d.c. signal, even to the collector of Q15, is demodulated audio signal.

In Figures 1, 2 and 3 the following are PNP-transistors: Q5, Q10, Q14 and Q15. All other transistors are NPN-transistors. Regarding the separation of "on-the-integrated-circuit-chip" components and "off-the-chip" or "outboarded" components in Figure 1, this is indicated by the various pads, such as P2 or P5; however, the following is helpful. All transistors and diodes are on the chip. All resistances are on the chip, except the following: the 27K resistor contained in the FM tuned circuit 18; the 100K potentiometer and 22K resistor which appear at the input to the audio amplifier 13. All capacitors, inductors and transformers are off-the-chip. Figure 1 employs the convention, customary in radio receiver manufacturers' practice, that resistance values are presumed to be expressed in ohms, unless indicated as K (kilohms); further that capacitance values (unless otherwise indicated) greater than one are in picofarads, and less than one are in microfarads.

In Figure 1, components shown to be returned to earth, are so returned to: (1) to an in-common on-the-chip earth point or line (not shown), for on-the-chip components; and (2) to an in-common off-the-chip earth point or line (not shown) for off-the-chip components. The on-the-chip earth line and off-the-chip earth line are joined at a pad (not shown) similar to pad P5.

The detailed description of Figure 1 will now be resumed.

The radio receiver performs the conventional functions. The input signal is converted to one of a pair of intermediate frequencies in the AM-FM converter 11. The FM section of the converter is normally provided with an external connection for a whip antenna or other suitable FM antenna. The AM section of the converter needs no external provision for signal reception since a ferrite element contained in the tuning unit normally

provides adequate signal pick up. The FM section produces an output at a fixed intermediate frequency, conventionally 10.7 MHz, while the AM section produces an output at a fixed intermediate frequency, conventionally 455 KHz. Depending upon the FM or AM mode selection an AM or FM signal is applied to the IF amplifier for signal separation and further amplification. Selection may be accomplished by another switch-arm (contained in the converter 11) of the mode selection switch 26. The last stage of the IF amplifier, shown in the circuit diagram of Figure 1, couples the amplified signal to the AM (19) and FM (18) filters at the detector input. The remainder of the electrical circuitry of Figure 1 is allocated to the detection function, the provision of an automatic gain control voltage on AM, an automatic frequency control voltage on FM and audio preamplification. After preamplification, detected signals are coupled to the audio amplifier 13 and loudspeaker 14.

The last stage of intermediate frequency amplification comprises the differential transistor pair Q11, Q12 together with a stabilized emitter current supply. The signal derived from the IF amplifier stages contained in the block 12 is applied "across" the bases of Q11 and Q12, i.e. providing push-pull IF signals to the bases of Q11 and Q12. Either way the bases of Q11 and Q12 should have the same d.c. potential, since their emitters are the same d.c. potential. The amplified output is derived from the collector of Q12 which is coupled to the pad P1. The pad P1 is one input connection point to the detector filters 18, 19. The collector of Q11 is returned to the 6 volt B+ bus 15. The emitters of Q11, Q12 are joined and provided with a constant emitter current ground return.

The current source for Q11, Q12 comprises transistors Q13, Q14, diodes D1, D2, D3, and sundry resistances. The constant emitter current is provided from the collector of Q13 whose emitter is led to ground through a 100 ohm resistance (20) and whose base emitter voltage is established by a reference coupled to its base. The reference for Q13 is established by a second current source including transistor Q14 whose collector is connected to the base of Q13 and returned to ground through a diode (D1) and resistance (17) in series. The emitter of Q14 is led through a current stabilizing (2.6K) resistor (21) to the B+ bias source. The base potential of Q14 is established at approximately two diode drops (D2+D3) below the B+ as a diode current level established by a resistance 16 returning the diodes to ground. The diodes D2 and D3

and resistance 16 thus establish the collector current of Q14 by V_{be} control, and in turn the current in serially connected diode D1 and resistance 17. The current in diode D1 and resistance 17 is then replicated—also by V_{be} control; for the purpose of such replication and of V_{be} control, the resistance 17 is given the same value as the resistance 20, namely 100 ohms. The replication occurs in transistor Q13 which provides a stabilized emitter current for Q11, Q12. The current setting is typically at around 200 microamperes.

The signal supplied by the IF amplifier is applied to the AM and FM filters (19, 18 respectively) before application to the AM-FM detector comprising transistor pair Q1, Q2. The filters provide further channel separation and phase shift functions essential to the detection process. The differential transistor pair Q1, Q2 are used in both AM and FM detection. More specifically, the filters (19, 18) apply a filtered IF signal in two different phases to the bases of the differential transistor pair Q1, Q2. The pads P1 and P2 are connected respectively to the input and output connection points of the AM and FM filters while the B+ bus 15 is connected via a pad P5 to the "common" filter connection points. The common connection also completes a current path from the collector of IF amplifier transistor Q12 to B+. The FM filter is a double tuned circuit as shown at 18 having a parallel resonant tank circuit at the input and a parallel resonant tank circuit at the output, capacitively coupled by capacitor 34 to produce a 90° phase shift at resonance. The capacitor 34 is normally selected to produce a slight overcoupling beyond critical to reduce audio distortion.

The FM filter is resonant at 10.7 MHz and has an input connection tapped on the input tank inductor. The AM filter 19 consists of a transformer having a tuned primary, also with a tapped input connection, and an untuned secondary with a phase inverting output connection. The tapped portions of the FM and AM input windings are thus serially connected between the pad P1 and the B+ bus and the output windings of the FM and AM filters are serially connected between the pad P2 and the B+ bus. The critical or overcritical coupling, and the 90° degree phase shift in the FM filter 18, are achieved by virtue of the fact that the parallel resonant output tank circuit is shunted by a 27K resistance, the discussion given so far does not yet take into account the effects of loading both parallel resonant circuits of the FM filter 18; the loading effects are relatively small, but beneficial as regards AFC performance, i.e. when the radio receiver

has not been exactly tuned in manually, but is being "pulled in" by the AFC action.

The circuitry involved in AM detection is illustrated with some simplification in Figure 2. It includes the AM filter 19, the transistor pair Q1, Q2 performing the detection function, and the audio preamplifying transistors Q3, Q5, a constant current source 25 (Q4 of Figure 1) and sundry resistances and capacitances. The AM tank circuit 19 is shown with the input tap connected to the base of Q1 and the phase inverting output connection of the secondary connected to the base of Q2. The omission of the FM windings from the AM equivalent circuit is justified by the negligible impedance of the 10.7 MHz transformer at 455 KHz. The collectors of Q1 and Q2 are joined together and coupled to B+ bus 15 which is also the "common" RF connection of the primary and secondary windings of AM filter 19. The emitters of Q1, Q2 are joined together. As will be explained, the circuit configuration produces full wave rectification of the AM signal at the emitters of Q1, Q2, functioning in a peak detection mode.

The detected output is preamplified in two following audio amplification stages. The first stage comprises the transistor Q3, connected in a high input impedance emitter follower configuration. Transistor Q3 has its base coupled to the emitters of Q1, Q2, its collector directly connected to the positive bias source 15 and its emitter coupled to ground through a constant current source 25 (comprising transistor Q4). The output derived from emitter follower Q3 is then applied to the base of transistor Q5 of the second amplifying stage. Transistor Q5 is connected in base input, emitter common configuration with its emitter led through a biasing resistance 22 to the B+ bus and its collector led through resistance 23 to ground. The amplified output signal appears at the collector of Q5. An RC network comprising resistance 23 and capacitor 24, connected between the collector of Q5 and ground, filters out any remaining components of intermediate frequency or higher harmonics. The amplified AM signal appearing at the collector of Q5 is now ready for final audio amplification. After further filtering, it is also ready for use as an automatic gain control voltage for the IF amplifier.

The current source 25, noted above, also participates in AM-FM mode selection. As illustrated in Figure 1, the source 25 comprises the transistor Q4 having its collector connected to supply current to the emitter of Q3 and its emitter returned to ground through a resistance 22. A mode setting switch 26 connected to pad P3 provides a positive 1.2 volt base bias to Q4

in the AM position and a 0 volt base bias in the FM position. The mode setting switch 26 thus allows Q4 to supply a substantial current to Q3 during AM operation but during FM operation reduces the current to Q3 substantially to zero.

AM detection is by full wave rectification in a peak detection mode. Waveforms describing the rectification process are illustrated at 27, 28, 29 and 30 of Figure 2. A first sinusoidal waveform 27 at IF frequency is applied to the base of Q1. A second sinusoidal waveform 28 at IF frequency, but of opposite phase to the waveform 27, is applied to the base of Q2. This opposing phase relationship is provided by reversal of the transformer output connections in the filter 19, as previously noted. The emitter current of Q1 and Q2 is held to a very low value by drawing its current from the base of Q3. This low current level is achieved by establishing the emitter current in emitter follower Q3 at about 170 microamperes corresponding to a base current of about 2 microamperes (depending upon the current gain of transistor Q3). If the signal goes negative on the base of one transistor of the differential pair (Q1, Q2), that transistor is cut off. If the signal goes positive, that transistor conducts at the current level available from the base of Q3. Thus, during the period that the base of Q1 is positive, a current may flow in the common emitter path and during the period that the base of Q2 is positive, a current may flow in the common emitter path. Thus, assuming a low impedance resistive load, a full wave rectified current reflecting the greater of the two signal voltages applied to the bases of Q1, Q2 will be produced in the common emitter path as represented by solid line waveform 29.

Detection occurs, however, in a peak detection mode, achieved by making the detector output circuit of high impedance and allowing appreciable stray capacity. The stray capacity results primarily from the collector-base capacitor of Q3 and normally is of the order of 3 picofarads. Under these conditions, the conduction periods required to charge the stray capacity to the peak values of the applied input voltage are short and confined largely to near the peaks of the sinusoidal input voltage. The short charging waveforms are interspersed with long and more gradual discharging waveforms. The peak detection voltage is illustrated by dotted waveform 30 in Figure 2. This waveform contains the audio signal modulation. The RC filter 23, 24 then removes the higher frequency harmonic terms and any traces of the IF carrier from the audio signal.

The circuitry involved in FM detection is

illustrated in a simplified form in Figure 3. It includes the FM filter 18; the transistor pair Q1, Q2, the transistor pair Q8, Q9 in a non-inverting modified differential amplifier configuration, and the base input, emitter common output amplifier Q10. The foregoing circuits convert the FM signal into variable width pulses, whose widths are proportional to the instantaneous frequency deviation of the signal, and which after integration contain the audio signal in the normal amplitude format. With suitable de-emphasis, the original audio modulation of the FM signal is obtained.

The FM filter 18 applies the signal to the transistor pair Q1, Q2. The input tap to the input resonant circuit of the filter is directly connected to the base of Q1. The output filter connection, which is phased at 90° (at resonance) with respect to the input drive, is directly connected to the base of Q2. The omission of AM windings from the FM equivalent circuit is justified by the low impedance properties of the 455 KHz AM transformer at 10.7 MHz. As in Figure 2, the collectors of Q1, Q2 are joined together and coupled to the B+ bus which is also the common RF connection for the input and output tank circuits of the FM filter. The emitters of Q1, Q2 are joined together and in the FM mode are supplied current from the collector of current source 33 (transistor Q6). The emitters of Q1, Q2 are at the point at which a waveform 36 having variable width negative going portions is produced. These negative going portions are subsequently converted to variable width rectangular pulses whose widths are proportional to the instantaneous frequency deviation.

The waveform 36 is produced in Q1, Q2 in the following manner. The FM filter 18 applies waves to the bases of Q1, Q2 which have a phase separation of 90° for zero frequency deviation. The waveform 31 (shown in Figure 3) is the input waveform from the input resonant circuit supplied to the base of Q1 and the waveform 32 is the output waveform from the output resonant circuit supplied to the base of Q2. The current levels in Q1, Q2 are set at about 130 microamperes by the constant current source 33 from which they derive their current. They are also arranged to operate linearly in respect to the input signal applied to their respective bases (i.e., no rectification by stray capacity). By virtue of the positive rectification action, the voltage output of the emitter followers follows the more dominant (higher) of the two input voltages. The "more dominant" voltage output characteristic, which is shown at 36 and which assumes linearity in the input characteristic, is seen to have a relatively high and broad double peaked positive

going portion and a shallower and narrower pointed negative going portion. The negative going portion, assuming a zero frequency deviation, is approximately 90° wide at the zero crossing, corresponding to a negative 1/4 duty cycle, and a positive 3/4 duty cycle.

At other than zero deviation, the output waveform will have a negative going portion that will be more or less than 90° as a function of the phase versus frequency characteristic of the FM tuned circuit. Assuming that capacitor 34 provides critical (or slightly over critical) coupling between the two resonant tank circuits, the amplitude waveforms will be as shown at 50 (or 51), and the phase will vary as shown in curve 38 (or 39) of Figure 4 from about 65° to 70° for maximum negative frequency deviation to 110° to 115° for maximum positive frequency deviation. During the interval that both signals applied to the bases of Q1, Q2 are negative, a sharp or "peaked" negative going portion of waveform 36 is produced at the emitters of Q1 and Q2. The width of the negative going portion at zero crossing is determined by the mutual phase displacement of the two applied waveforms. When the waveforms 31, 32 are at minimum mutual displacement (65°—70°), the peaked negative going portion is widest (being 110°—115°), and when the waveforms 31, 32 are at maximum mutual displacement (110°—115°), the peaked negative going portions are narrowest (being 65° to 70°). With audio modulation, the frequency deviation will vary between ±75 KHz for maximum audio intensity, and the peaked negative going portions of waveform 36 will be produced at the intermediate frequency rate having angular widths which vary 20° to 25° above and below an average of 90°. Larger phase variations are possible if higher audio distortions (over 1%) are acceptable.

In addition to having a variable width as a function of the frequency deviation, the peaked negative going portions of the waveforms vary in amplitude. In the upper limit (i.e. 180° phase shift) a wave resembling full wave rectification is produced, in which the amplitude of the negative going portion is zero. In the lower limit (i.e., 0° phase shift), the amplitude of the negative going portion is essentially full amplitude. At 90° phase separation, the amplitude is 71% of full amplitude and a variation of ±22.5° produces an amplitude range of 38%—92% of the full amplitude. Accordingly, in applications where second order harmonics resulting from the undesired amplitude variation should be avoided, the output of Q1, Q2 should be

processed by a zero crossing detector which removes the amplitude variations.

The differential amplifier Q8, Q9 ideally provides zero crossing detection by providing a high gain for small signal levels, with limiting action occurring before normal signal levels are reached. The idealized output waveform of Q8, Q9, neglecting integrative effects, is shown at 37.

The differential amplifier achieves a controlled high gain by use of both a regenerative and a degenerative feedback loop. The emitters of Q8, Q9 are joined and receive current from current source 35 (transistor Q7). The collector of Q8, which is coupled to the base of Q9 in the forward gain path, is coupled to the B+ bus through diode D4. The collector of Q9 is coupled to the B+ bus through resistance 27 in series with diode D5. The connection of the collector of Q8 to the base of Q9 transfers the signal from Q8 to Q9, and the common emitter coupling from Q9 back to Q8 completes the regenerative feedback path which is around both stages. The negative feedback path is from the collector of Q9 back to its base. The negative feedback path is from the cathode of diode D5 in the collector load of Q9 through a resistance 28 connected to the base of Q9 and around the second stage only. It tends to stabilize the gain of the amplifier. The signal output of the differential amplifier is derived from the collector of Q9. This arrangement gives a maximum gain of about 10 for small signals, the gain decreasing rapidly as limiting occurs for both positive and negative signal excursions.

The limiting action in Q8, Q9 is achieved by setting fixed positive and negative output states (limiting levels) about the zero signal output states (static level 136) and by providing an adequately large input signal and adequate gain to cause the output to attain these limiting levels at normal signal excursions. The current source 35 provides approximately 300μA of current for Q8, Q9, while the current source 33 provides about 130μA of current for Q1, Q2. In the zero signal state, i.e. no IF signal present, Q1 and Q2 conduct equally (65μA each), and Q8 conducts about three-quarters (225μA) of the current from source 35 while Q9 conducts about one-quarter (75μA) of the current from source 35. Since the emitters of Q8, Q9 are joined, this current division is achieved by applying a voltage to the base of Q8 which is larger (by approximately 35 mV) than the voltage applied to the base of Q9. The voltage applied to the base of Q8 is the static level voltage 136 i.e. the voltage at the emitters of Q1 and Q2 at this normal current setting (130μA). The lesser voltage applied to the base of Q9 is substantially (70%) equal to

the drop produced by the current passing through the diode D4 which is connected between the B+ bus 15 and the base of Q9. With a signal of positive polarity present on the base of either transistor Q1 or Q2, a corresponding increase in voltage will appear at their common emitters. Applied to the base of Q8, this increase will cause Q8 to conduct more strongly, increasing its drop in diode D4 and lowering the voltage applied to the base of Q9. A lowered base voltage applied to Q9 will reduce the collector current of Q9 and cause an increase in collector voltage of Q9. In the resultant limiting condition, Q8 becomes fully conductive and Q9 becomes non-conductive. Applied to the base of Q10, this increase in collector voltage of Q9 tends to reduce the current in Q10 toward cut off.

With both signals applied to the bases of Q1, Q2 of negative polarity, the converse occurs and Q10 is driven into relatively high conduction. This is so because when the common emitters of Q1, Q2 are depressed, Q8 will conduct less strongly and Q9 will conduct more strongly causing a reduction in voltage at the collector of Q9. In the resultant limiting condition, Q8 becomes nonconductive, Q9 becomes conductive and the current in Q10 increases.

In either of the above cases, very substantial limiting occurs when the input signal to the base of Q8 exceeds 50 or 60 millivolts peak. When the applied signal (input to the base of Q1 or Q2) is large in respect to this Figure, as it should be (typically it is 1/2 volt peak to peak), the output signal of Q9 is essentially a rectangular pulse train as shown at 37 in Figure 3. Thus, the differential amplifier (Q8, Q9) eliminates amplitude variation in the positive state and in the negative state of the signal train 36, and steepens the transition between states.

Assuming no integration by parasitic capacitances, the output pulses appearing at the collector of Q9 would contain the succession of constant amplitude, nearly rectangular pulses occurring at the intermediate frequency rate shown at 37. There is, however, some integration performed by capacitance appearing in the load circuit of the differential amplifier Q8, Q9 as a result of the input impedance of the following amplifier Q10. The capacitive effect is insufficient to prevent resolution of the individual pulses as they appear at the collector of Q9. In the degenerative feedback loop fed from the collector of Q9, it merely reduces the bandwidth of the feedback signal. The bandwidth reduction is small and permits the degenerative loop to function with only slightly reduced speed. The regenerative loop on the other hand, is isolated from this capacitive

loading and allows rapid switching from one state to the other. The actual output pulses of Q9 thus experience a reduction in rectangularity consistent with some roll-off in the amplification process.

The roll-off is easily determined. The load circuit for the differential amplifier (Q8, Q9) consists in part of the base emitter capacitance of the succeeding PNP transistor amplifier stage Q10 and a small (1K) emitter load resistance 22B connecting the emitter of Q10 to B+. The base to emitter capacitance of Q10 is several picofarads since it is a laterally formed PNP transistor. Thus the roll-off is in a doublet form, never introducing more than the 1K emitter load resistance 22B in shunt with the collector load resistance 127 of Q9 (3.9K) at even the highest frequencies.

In addition to the foregoing, two other integrative effects are present and associated with the transistor amplifier Q10. The first is attributable to the drift time required for the carriers in the laterally formed PNP transistor to reach the collector and the second is the integrative effect produced by the RC network 23, 24. The collector of Q10 from which the output signal is derived is connected to RC network 23, 24 at the same point as the collector of Q5 (which is quiescent in the FM mode). The PNP transistor Q10 has a relatively low frequency cut-off of several hundred kilocycles. Thus, since the individual pulses of the 10 megacycle IF rate can no longer be resolved, low frequency information is recovered, based on the average pulse width or duty cycle of the pulses. This low frequency information is the audio information in the FM signal. The RC network 23, 24 is selected to provide the required 75 μ sec de-emphasis to reconstitute the original modulating audio signal.

The schematic diagram of Figure 1 combines the AM and FM circuitry and adds current supply and control circuit details omitted in Figures 2 and 3. For instance, the equivalently represented current source 25 of Figure 2 is shown as a transistor Q4 with a base connection to the mode switch 26 and an emitter connection to ground through resistance 22 in Figure 1. There are three additional current sources in Figure 1 operative in the FM mode and inoperative in the AM mode in consequence of the setting of the mode switch 26. Current source 33 of Figure 3 is shown as the transistor Q6 of Figure 1 having its collector returned to the emitters of Q1, Q2, its base led to the pad P4 to which a fixed bias supply 1.2 volts and filtering is applied and its emitter led through a resistance 43 to an ancillary

connection point at the left terminal of a second-resistance 44 coupled to the pad P3 at the mode switch 26. Current source 35 of Figure 3 is the transistor Q7, having its collector coupled to the emitters of differential amplifier Q8, Q9, its base coupled to the pad P4 (+1.2 volts) and its emitter coupled through a second resistance 45 to the left terminal of resistance 44.

A current source in accordance with the invention is shown at 129.

An AFC-AGC transistor stage Q17 is provided, not shown in either Figure 2 or 3; it serves to adjust the level of AGC or AFC output from the current source 129 as a function of the FM or AM mode setting. The AFC-AGC stage Q17 has its base returned to the pad P4 (+1.2 volts), its emitter led through a resistance 46 to the left terminal of resistance 44 and its collector led through a Veb current reference comprising serially connected diode D6 and resistance 48 to the B+ bus.

The AFC-AGC stage Q17 increases the output current of the AGC, AFC amplifier or current source 129 in the FM mode over that in the AM mode. The emitter of Q17 is connected to the aforementioned "left" terminal of resistance 44, whose "right" terminal is led to the pad P3 and thence via mode switch 26 to earth in FM mode, and to a +1.2 volt bias supply in AM mode. Also, the base of Q4 is connected to the pad P3, and is therefore placed at earth potential in FM mode, and at +1.2 volts in AM mode. The resistances 46, 43, 45 and 44 thus form a resistive connection, with resistance 44 in common to, and respective resistances 46, 43 and 45 being individual to, the emitter circuits of Q17, Q6 and Q7 respectively. In the earthed, FM-position of the mode switch 26, the transistors Q17, Q6 and Q7 are rendered conductive, but Q4 is cut off and with it Q3 and Q5 are cut off. With Q6 conducting, Q1 and Q2 are caused to operate as "selection circuit" as previously described. With Q7 rendered conductive, Q8 and Q9 are enabled to operate as zero crossing detector, and the resultant collector potential of Q9 enables conduction of Q10 as previously described.

With mode switch 26 in the AM position, +1.2 volts is applied to the right terminal of resistance 44—this cuts off Q17, Q6 and Q7 as their bases are also at +1.2 volts—and to the base of Q4, rendering Q4, and with it, Q3 and Q5 conductive, to operate as AM audio pre-amplifier as previously described. Although Q6 no longer conducts, Q1 and Q2 are enabled to operate as full-wave rectifier as previously described. The cut-off of Q7 also cuts off Q8, Q9, and with them, Q10.

From now on, concentration will be on Q17 and indeed on the entire AFC-AGC amplifier or current source 129, which further includes the mentioned diode D6 as well as AFC-AGC amplifier transistor Q16, and the current source output transistor Q15, which is PNP, whereas Q16 and Q17 are NPN. The fact of conduction of Q17 in FM-mode, and its non-conduction in AM-mode, results in higher output current of Q15 in FM-mode than in AM-mode, which causes the IF amplifier 12 to exhibit higher gain in FM-mode than in AM-mode, and also subjects the IF amplifier 12 to automatic gain control in AM-mode.

The AGC, AFC amplifier or current source 129 comprises the NPN transistors Q16 and Q17, the output PNP transistor Q15, and the mentioned diode D6. The current source is primarily a current-amplifier, or input-voltage to output-current amplifier, with dynamic AFC or AGC voltage-signal input received at the base of Q16, static signal input to the emitter of Q17 (via resistances 46 and 44), and composite static and dynamic current output delivered from the collector of Q15 via the primary bus 118 to the "load" on the current source, namely IF amplifier 12 and AM-FM converter 11. The current source 129 is, considered at the collector of Q15 (primary bus 119), a current-oriented rather than voltage-oriented device; its output voltage depends on the impedance presented to it by its load, and as explained in McFadyen I, the loading in FM-mode differs from the loading in AM-mode. However, with a given load, either in FM-mode or AM-mode, output current on primary bus 118 and output voltage (with respect to earth) on bus 118, go hand in hand, both increasing and decreasing together, and in this sense it will be convenient to consider the unit 129 also as an AGC, AFC voltage amplifier. The current source 129 is designed to provide an amplified AGC voltage in the AM mode and an amplified AFC voltage in the FM mode. The input stage of the control amplifier includes a transistor Q16, whose base is coupled via line 165 to both the collector of Q5, at which appears the detected AM signal containing the dynamic AGC signal and demodulated audio, appears when the receiver is in the AM mode, and to the collector of Q10, at which appears the detected FM signal containing the dynamic AFC signal and demodulated audio, when the radio receiver is in the FM mode. The emitter of Q16 is led to ground through resistance 47 and the collector is led through the current reference, comprising resistance 48 and diode D6, to the B+ bus. The output stage of the control amplifier or current source 129 includes

PNP transistor Q15, whose base is connected to the collector of Q16 and to the V_{be} reference (D6, 48) and the collectors of Q16 and Q17, its emitter being led through resistance 49 to the B_+ bus. The values of resistances 48 (400 ohms) and 49 (50 ohms) are in the ratio of 8:1 for the same reasons as given in McFadyen I, namely to establish a substantially 8:1 ratio of emitter current of Q15, to current conducted by diode D6. The potential established at the base of Q15 is determined by the mode setting—Q17 conducts in FM-mode, but is cut off in AM-mode—and on the magnitude of the dynamic AFC or AGC signal on line 165. The so established base-potential of Q15 in turn determines the base current of Q15, of which the collector current of Q15 (on primary bus 118) is an amplified version. The base current of Q15 combines itself with the current drawn by the diode D6; the combined current is distributed as the collector currents of both Q16 and Q17 in FM-mode, but in AM-mode the combined current is the collector current of solely Q16, since Q17 is cut off in AM-mode.

The amplified control voltage supplied from the AM and FM detectors and amplified in the control amplifier 129 is used to control the IF amplifier 12 and the AM, FM converter 11. In the AM setting, the gain of the IF amplifier is controlled by the use of current control of the several stages. Also, the gain of the converter 11 and any RF stages may be in AM mode similarly subject to this or another mode of gain control. In the FM setting, the current level is boosted sufficiently high in the IF amplifier so that gain is essentially unaffected by any changes in the current supplied by Q15 while a variable voltage is applied to the FM local oscillator. The FM local oscillator is therefore selected so that its frequency characteristic is voltage dependent and voltage dependent in a sense to achieve correction of any drift, and to correct by pull-inaction, for manual dial tuning error.

The foregoing FM detector is preferable to the conventional circuits normally used in integrated circuit fabrication. In integrated circuit or discrete form, the heart of the detector, the differentially connected emitter follower pair Q1 and Q2 facilitates low distortion in the detection process. In comparison to the known two and four quadrant multiplier detection circuits, which introduce 30° to 50° differential phase shift between the signal applied to the lower rank and the quadrature signal applied to the upper rank, the present arrangement introduces no additional differential phase shift. Since the differential phase is signal level

sensitive, it causes 5° to 10° variation in phase shift in the cited multiplier arrangement. This cause of distortion is eliminated in the present arrangement.

In addition, the present detection arrangement presents a near optimum loading relationship to the tuned circuit. It presents a minimum of loading to the tuned circuit; one that is balanced between the input tank circuit and the output tank circuit; and finally, loading that is essentially constant and independent of signal level. In FM demodulators, the effective Q of the tuned discriminator circuits is reduced by the loading introduced by the active detection elements. Since herein the loading is not produced by simple diodes, but rather by transistor input junctions, the loading in the present arrangement is reduced by a factor corresponding generally to the betas of the transistors. Since the loading is relatively small, the resonant circuits of the FM filter may operate at higher than normal Qs. Since the loading is small, there is a minimum of de-tuning at all signal levels. In addition, due to the shared nature of the conduction cycle, in which the transistors Q1 and Q2 each equally share the conduction intervals in positive or negative phases, the loading effect on both tank circuits is equal. Thus, to the extent that there is load, there is equality between the input and output filters and they may be tuned for normal signal levels. In addition to this equality between input and output circuit loading, the loading on the tuned circuit remains essentially constant since the emitter current, and consequently the base currents, are held to be substantially constant over time by the emitter current source (33).

While the embodiment described has been illustrated using conventional filters for AM and FM operation, it should be understood that other selections may be made. For instance, one may use a delay line for FM operation which is long enough to produce the requisite phase slope. Normally, at the standard frequencies used in FM, this approach is prohibitively expensive. However, at higher frequencies or when other modulating standards are employed, the delay line approach is often practical. In addition, one may use ceramic resonators or in the case of the FM filter 18, one may employ an initial load circuit which is untuned followed by a single tuned secondary. One could also employ surface wave devices for these same purposes.

In the preferred receiver circuit, the detectors Q1, Q2 are operated linearly, typically at 130 microamperes, and produce a variable width waveform whose zero

crossings are spaced in linear proportion to the frequency deviation of the signal. A zero crossing detector follows the detection diodes and senses the zero crossings and produces a rectangular pulse waveform whose zero crossings match the zero crossings of the waveform derived previously. If the zero crossing detector is not employed, frequency discrimination is still produced by the emitter-follower pair. The circuit, however, is subject to sensitivity to amplitude modulation as well. Thus, if one looks at the area of the curve in the negative going direction of Figure 3, one will see that both the width of the negative going region and also its height are varied. If the input waveform is linear through the frequency domain, then this effect will produce a second order term which would normally appear as detection distortion. However, it is possible to shape the bandpass characteristic of the filter, so that the amplitude falls off suitably (by using a narrower band filter) to compensate for this increased second order term in the detector. Thus, considering both the effect of the filter and of the detection circuit, the amplitude nonlinearity may be compensated out without the need for a following limiting amplifier. However, in certain narrow band applications, or those in which a small amount of distortion is unimportant, compensation may be unnecessary.

The amplitude and phase response of the filter 18 is preferably adjusted to extend the range of linearity of the demodulator. In particular, the two tuned circuits are overcoupled to produce the extended phase response (39) illustrated in Figure 4. The foregoing adjustment leads to a distortion figure of about one-fourth of one percent at optimum overcoupling.

The zero crossing detector may take other forms than the one herein illustrated. In the present preferred configuration, the device has a high gain for low signal levels and is very rapidly driven into a limiting condition by signals of either polarity at 60 or 70 millivolts above or below the bias point. Since the device is normally driven with 500 millivolt peak to peak signals, the normal signal levels achieve essentially hard limiting. Other forms of zero crossing detectors may be employed, including standard regenerative amplifiers. The zero crossing detector amplifier should be nonlinear therefore so as to achieve saturation at low signal excursions of either polarity and when the signal is removed should have no hysteresis so that the amplifier quickly returns to its original bias point.

The detector uses separate audio preamplifier stages, Q5 and Q10 for AM and FM respectively, but utilizes the same

final RC network comprising the resistance 23 and the capacitance 24. These values are selected to provide the correct de-emphasis for the usual frequency modulation signal and in many respects, it approximates the desired frequency response for the AM receiver.

Reference is made to our co-pending Patent Application No. 13415/75 (Serial No. 1,511,041) from which this application has been divided and which discloses and claims an FM detector as disclosed herein, and to our Application No. 50660/77 (Serial No. 1,511,042) also divided out of 13415/75 (Serial No. 1,511,041) which discloses and claims an IF amplifier as disclosed herein.

WHAT WE CLAIM IS:—

1. A current source comprising an output transistor of a first conductivity type for providing at its collector a d.c. output current, a direct coupled amplifier controlling said output transistor, and first and second inputs to said amplifier, the arrangement being such that a d.c. signal applied to the second input determines the static d.c. level of the output current and the dynamic level of the output current is determined by a signal supplied to the first input, the source further including a power supply line to which is connected, via a first resistance, the emitter of the output transistor, the current source further comprising, connected between the base of the output transistor of the current source and the power supply line a series combination of (1) a semiconductor diode device which is poled to conduct current in the same direction as the direction of emitter current flow of the current source's output transistor, and of (2) a second resistance, said series combination, in operational use, serving to conduct a current with which is combined the base current of the output transistor, that base current being amplified by the output transistor, the magnitude of the latter combined current and hence of the output transistor's base current being determinable by the potential established at the output transistor's base, said direct coupled amplifier including a first and a second additional transistor, each of a second conductivity type opposite to the first conductivity type, the collectors of the first and second additional transistors being connected together and to the base of the output transistor, the base of the first additional transistor constituting the first input of the current source, and the emitter of the second additional transistor constituting said second input being connected to a resistive connection—itsself comprising a resistance having an end connected to the latter emitter—the latter



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crossings are spaced in linear proportion to the frequency deviation of the signal. A zero crossing detector follows the detection diodes and senses the zero crossings and produces a rectangular pulse waveform whose zero crossings match the zero crossings of the waveform derived previously. If the zero crossing detector is not employed, frequency discrimination is still produced by the emitter follower pair. The circuit, however, is subject to sensitivity to amplitude modulation as well. Thus, if one looks at the area of the curve in the negative going direction of Figure 3, one will see that both the width of the negative going region and also its height are varied. If the input waveform is linear through the frequency domain, then this effect will produce a second order term which would normally appear as detection distortion. However, it is possible to shape the bandpass characteristic of the filter, so that the amplitude falls off suitably (by using a narrower band filter) to compensate for this increased second order term in the detector. Thus, considering both the effect of the filter and of the detection circuit, the amplitude nonlinearity may be compensated out without the need for a following limiting amplifier. However, in certain narrow band applications, or those in which a small amount of distortion is unimportant, compensation may be unnecessary.

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The detector uses separate audio preamplifier stages, Q5 and Q10 for AM and FM respectively, but utilizes the same

final RC network comprising the resistance 23 and the capacitance 24. These values are selected to provide the correct de-emphasis for the usual frequency modulation signal and in many respects, it approximates the desired frequency response for the AM receiver.

Reference is made to our co-pending Patent Application No. 13415/75 (Serial No. 1,511,041) from which this application has been divided and which discloses and claims an FM detector as disclosed herein, and to our Application No. 50660/77 (Serial No. 1,511,042) also divided out of 13415/75 (Serial No. 1,511,041) which discloses and claims an IF amplifier as disclosed herein.

WHAT WE CLAIM IS:—

1. A current source comprising an output transistor of a first conductivity type for providing at its collector a d.c. output current, a direct coupled amplifier controlling said output transistor, and first and second inputs to said amplifier, the arrangement being such that a d.c. signal applied to the second input determines the static d.c. level of the output current and the dynamic level of the output current is determined by a signal supplied to the first input, the source further including a power supply line to which is connected, *via* a first resistance, the emitter of the output transistor, the current source further comprising, connected between the base of the output transistor of the current source and the power supply line a series combination of (1) a semiconductor diode device which is poled to conduct current in the same direction as the direction of emitter current flow of the current source's output transistor, and of (2) a second resistance, said series combination, in operational use, serving to conduct a current with which is combined the base current of the output transistor, that base current being amplified by the output transistor, the magnitude of the latter combined current and hence of the output transistor's base current being determinable by the potential established at the output transistor's base, said direct coupled amplifier including a first and a second additional transistor, each of a second conductivity type opposite to the first conductivity type, the collectors of the first and second additional transistors being connected together and to the base of the output transistor, the base of the first additional transistor constituting the first input of the current source, and the emitter of the second additional transistor constituting said second input being connected to a resistive connection—itsself comprising a resistance having an end connected to the latter emitter—the latter



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resistive connection being alternatively connectible in operational use of the current source, either to a primary reference point or line so as to render said second additional transistor conductive and thereby determine one static d.c. level of the current source's output current, or to a line or point which in operational use is at a steady d.c. potential sufficiently high to cut off said second additional transistor, and thereby determine another static d.c. level of the current source's output current, and the base of the second additional transistor being connected to a secondary reference point or line.

2. A current source as claimed in Claim 1, wherein the values of the first and of the second resistance are in a predetermined proportion.

3. A current source as claimed in Claim 1 or Claim 2, wherein integrated together are the respective transistors, resistances resistive connections, and semiconductor diode device.

4. A current source as claimed in any preceding claim, wherein the resistive connection at its end remote from the emitter of the second additional transistor, is connected to switching means operable to connect such remote-from-emitter end alternatively to the primary reference line, or to said point or line carrying d.c. cut off potential.

5. A current source as claimed in any preceding claim, wherein said d.c. cut off potential is provided, in operational use, by a source of secondary, d.c. bias potential.

6. A current source as claimed in Claim 1 and substantially as hereinbefore described with reference to, and as shown in, the accompanying drawings.

7. A current source as claimed in Claim 1, in combination with an FM-detector comprising,

(a) a source of frequency modulated signals of predetermined centre frequency,

b) phase shift means for producing a substantially linear change of phase with frequency through a range lying between successive even multiples of 90° ,

c) a differentially connected emitter follower pair comprising a pair of transistors, the collectors of both transistors being jointly coupled to a bias source, the emitters of both transistors being jointly coupled to ground through a load impedance, and the base of one transistor being coupled to said source without phase shift and the base of the other transistor being coupled to said source through said phase shift means to produce at the joined emitters an output waveform representing

the greater (more positive or less negative) of the two input waveforms and having zero crossing widths proportional to the phase separation of the input waves, said output waveform having a portion of one polarity which is broad and double-humped while having a portion of the other polarity which is narrow and single peaked, and

d) integrating means coupled to said load impedance for providing a time averaged waveform whose amplitude is proportional to the frequency deviation to obtain the original signal modulation, and means for connecting said time average waveforms to the said first input of the current source.

8. A current source as claimed in Claim 1, in combination with an FM-detector for use in an FM broadcast band radio receiver, said FM detector being of the type which is connectible to receive a first and a second frequency-modulated input-signal-train, both signal-trains having the same nominal centre frequency of FM-IF (intermediate frequency), the second input signal-train being a phase-shifted version of the first input signal-train, with the phase shift being substantially linear as a function of frequency through a range lying on either side of an odd multiple of 90° (the phase shift at zero frequency deviation of the input FM signal), the detector including means for combining the input signal-trains to produce an output signal-train having an waveform which comprises a succession of variable-width signals, the width variations being in accordance with the relative phase-displacement of the input signal-trains, means for integrating signals having the said variable widths, wherein the combining means is a "pass-the-most dominant-input-signal" selection circuit as herein defined, and a limiter, interposed between the selection circuit and the integrating means, which substantially symmetrically clips the output signals in the train obtained from the selection circuit, and produces a substantially rectangular wave pulse train containing pulses of width which is variable in correspondence with the width variations of the selection circuit output signal train, the integrating means actually integrating the rectangular pulse wave train to provide the demodulated signal, and means for connecting the demodulated signal to the said first input of the current source.

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