

ABSTRACT

A bias stabilization circuit for biasing the DC gate bias of a stabilized transistor is disclosed. The bias stabilization circuit may be comprised of a bias transistor that is fabricated concurrent with, and on the same chip as, the stabilized transistor. Preferably, the bias transistor and the stabilized transistor are fabricated physically close to each other and during the same process so that the electrical characteristics of the transistors are closely related. In a preferred embodiment, a drain of the bias transistor is connected to a load comprising a first resistor, a second resistor, and a third resistor. The drain of the bias transistor is connected through the third resistor to a junction between the first and second resistors. The first and second resistors are connected in series between a first supply potential and a reference potential. The gate and source of the bias transistor are connected together through a fourth resistor. The gate is also connected to a second supply potential that is derived from the first supply potential. The third and fourth resistors are fabricated together with the bias and stabilized transistors. By this configuration, if the operating characteristics of the stabilized transistor varies from chip to chip during fabrication due to process variations, or the supply



potentials vary, the bias transistor will compensate to maintain a substantially constant operating point of the stabilized transistor.

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