Abstract

METHOD FOR FORMING AN EXTENDED METAL GATE USING A DAMASCENE PROCESS

A method for forming an extended metal gate without poly wrap around effects. A semiconductor structure is provided having a gate structure thereon. The gate structure comprising a gate dielectric layer, a gate silicon layer, a doped silicon oxide layer, and a disposable gate layer stacked sequentially. Spacers are foremed on the sidewalls of the gate structure. A dielectric gapfill layer is formed over the semiconductor structure and the gate structure and planarized, stopping on the disposable gate layer. A first silicon nitride layer is formed over the disposable gate layer, and a dielectric layer is formed over the first silicon nitride layer. The dielectric layer is patterned to form a trench over the gate structure; wherein the trench has a width greater than the width of the gate structure. The first silicon nitride layer in the bottom of the trench and the disposable gate layer are removed using one or more selective etching processes. The doped silicon oxide layer is removed using an etch with a high selectivity of doped silicon oxide to undoped silicon oxide. A barrier layer is formed over the gate silicon layer, and a metal gate layer is formed on the barrier layer; whereby the metal gate layer has a greater width than the gate structure.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)