

CLAIMS

WHAT IS CLAIMED IS:

1. A system comprising:
at least one processor; and
5 a computer-readable storage device storing instructions which, when executed by the at least one processor, cause the at least one processor to:
receive an algorithm from an algorithm provider;
receive data from a data provider;
divide the algorithm into a first algorithm subset and a second algorithm
10 subset for separate and independent processing of respective data sets by the first algorithm subset and the second algorithm subset, wherein the first algorithm subset and the second algorithm subset, when combined, comprise the algorithm;
divide the data into a first data subset and a second data subset;
transmit the first algorithm subset and the first data subset to a first entity for
15 processing;
transmit the second algorithm subset and the second data subset to a second entity for processing, wherein the first entity processes the first algorithm subset with the first data subset and wherein the second entity processes the second algorithm subset with the second data, and wherein the first entity and the second entity
20 exchange interim partial results while processing the first algorithm subset with the first data subset and the second algorithm subset with the second data;
receive, from the first entity, a first partial result based on the first algorithm subset and first data subset and receive, from the second entity, a second partial result based on the second algorithm subset and the second data subset; and
25 determine a combined result based on the first partial result and the second partial result.
2. The system of claim 1, wherein the computer-readable storage device stores additional instructions which, when executed by the at least one processor, cause the at least
30 one processor to:

convert the algorithm into a Boolean logic gate set, wherein the first algorithm subset corresponds to a first Boolean logic gate subset of the Boolean logic gate set and wherein the second algorithm subset corresponds to a second Boolean logic gate subset of the Boolean logic gate set.

- 5 3. The system of claim 2, wherein the first Boolean logic gate subset and the second Boolean logic gate subset comprise AND gates and XOR gates.
4. The system of claim 1, wherein the algorithm provider comprises at least one first computing device and the data provider comprises at least one second computing device.
5. The system of claim 1, wherein the computer-readable storage device stores
10 additional instructions which, when executed by the at least one processor, cause the at least one processor to:
 send the combined result to the data provider and display a representation of the combined result.
6. The system of claim 1, wherein the computer-readable storage device stores
15 additional instructions which, when executed by the at least one processor, cause the at least one processor to:
 send the combined result to the algorithm provider and display a representation of the combined result.
7. The system of claim 1, wherein the algorithm is selected from a list of algorithms
20 provided by the algorithm provider.
8. The system of claim 1, wherein the algorithm is represented by one of a Boolean logic set, a neural network or an algebraic circuit.
9. The system of claim 1, wherein the computer-readable storage device stores
25 additional instructions which, when executed by the at least one processor, cause the at least one processor to:
 encrypt the algorithm and encrypt the data.
10. A method comprising:
 receiving, by at least one processor, an algorithm from an algorithm provider;

- receiving, by the at least one processor, data from a data provider;
- dividing, by the at least one processor, the algorithm into a first algorithm subset and a second algorithm subset for separate and independent processing of respective data sets by the first algorithm subset and the second algorithm subset, wherein the first algorithm subset and the second algorithm subset, when combined, comprise the algorithm;
- 5 dividing, by the at least one processor, the data into a first data subset and a second data subset;
- transmitting the first algorithm subset and the first data subset to a first entity for processing;
- 10 transmitting the second algorithm subset and the second data subset to a second entity for processing, wherein the algorithm provider processes the first algorithm subset and the first data subset and wherein the data provider processes the second algorithm subset and the second data subset, and wherein the first entity and the second entity exchange multiple interim partial results while processing the first algorithm subset with the first data subset and
- 15 the second algorithm subset with the second data;
- receiving, by the at least one processor, a first partial result based on the first algorithm subset and first data subset and receiving a second partial result based on the second algorithm subset and the second data subset; and
- determining, by the at least one processor, a combined result based on the first partial
- 20 result and the second partial result.

11. The method of claim 10, wherein the dividing of the algorithm into a first algorithm subset and a second algorithm subset further comprises:

- converting the algorithm into a Boolean logic gate set, wherein the first algorithm
- 25 subset is represented by a first Boolean logic gate subset of the Boolean logic gate set and wherein the second algorithm subset is represented by a second Boolean logic gate set.

12. The method of claim 11, wherein the first Boolean logic gate subset and the second Boolean logic gate subset comprise AND gates and XOR gates.

13. The method of claim 10, wherein the algorithm provider comprises at least one first
- 30 computing device and the data provider comprises at least one second computing device.

14. The method of claim 10, further comprising:
sending the combined result to the data provider and displaying a representation of the combined result.
15. The method of claim 10, further comprising:
5 sending the combined result to the algorithm provider and displaying a representation of the combined result.
16. The method of claim 10, wherein the algorithm is selected from a list of algorithms provided by the algorithm provider.
17. The method of claim 10, wherein the algorithm is represented by one of a Boolean
10 logic set, a neural network or an algebraic circuit.
18. The method of claim 10, further comprising encrypting the algorithm and encrypting the data.
19. A non-transitory computer-readable storage medium having stored therein instructions which, when executed by one or more processors, cause the one or more
15 processors to:
receive an algorithm from an algorithm provider;
receive data from a data provider;
divide the algorithm into a first algorithm subset and a second algorithm subset for separate and independent processing of respective data by the first algorithm subset and the
20 second algorithm subset, wherein the first algorithm subset and the second algorithm subset, when combined, comprise the algorithm;
divide the data into a first data subset and a second data subset;
send the first algorithm subset and the first data subset to a first entity;
send the second algorithm subset and the second data subset to a second entity,
25 wherein the first entity and the second entity exchange interim partial results while processing the first algorithm subset with the first data subset and the second algorithm subset with the second data;

receive a first partial result from the first entity based on the first algorithm subset and first data subset and receive a second partial result from the second entity based on the second algorithm subset and the second data subset; and

5 determine a combined result based on the first partial result and the second partial result.

20. The non-transitory computer-readable storage medium of claim 19, storing instructions which, when executed by the one or more processors, cause the one or more processors to:

10 convert the algorithm into a Boolean logic gate set, wherein the first algorithm subset corresponds to a first Boolean logic gate subset of the Boolean logic gate set and wherein the second algorithm subset corresponds to a second Boolean logic gate subset of the Boolean logic gate set.