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METHOD AND APPARATUS
PROVIDING HIGH SPEED
VIDEO SIGNAL LIMITING

5 This invention relates to limiters and particularly to high speed limiters suitable for use with wideband (i.e. video) signal sources.

 Precise limiting of fast rise-time narrow (e.g., less than 100 nano-Second) pulses of relatively low amplitude (e.g., <1 volt) 10 presents a technical challenge. It is especially true when the available hardware is limited by cost, board area or other construction considerations. The conventional limiters using diode, or Zener diode, junction or saturation characteristics of a transistor either do not work at all in the case of very narrow and small 15 amplitude pulses (e.g., 100 n-Second, 1 volt) or do not guarantee acceptable performance. Such pulses are commonly encountered, for example, in video signal processing circuits.

 As an example, it is common practice to apply peaking to luminance signals for improving the apparent sharpness of 20 image edges. Certain types of peaking circuits, however, create overshoots which are acceptable at most video signal levels but which may exceed 100 IRE levels for signals at or near peak white. Exceeding the peak white levels may, in turn, lead to undesired saturation or "blooming" effects and so it would be 25 desirable to limit or "clip" overshoots exceeding peak white levels. A particular problem in limiting pulses of short duration and relatively low amplitude is delayed response. Other applications in which fast pulse limiting action would be desirable include noise limiters in communications equipment, input signal conditioners 30 in analog to digital converters and so forth.

 The present invention is directed to meeting the need for a limiter suitable for general signal limiting applications and particularly well suited for applications, such as video signal processing, for limiting relatively fast pulses (e.g., in the nano- 35 Second region) which may be of relatively low amplitude (e.g., in the milli-Volt region).

A method, in accordance with the invention, for limiting an input signal, comprises coupling the input signal to an output terminal via the base emitter path of a first transistor; coupling a threshold signal to the output terminal via the base emitter path of a second transistor; applying a supply voltage to the collector electrodes of the first and second transistors; coupling the output terminal to a source of reference potential via a first resistor and to a selected one of the base and collector electrodes of the second transistor via a second resistor; and coupling a capacitor between the base and collector electrodes of said second transistor.

Pulse limiting apparatus, embodying the invention, comprises first and second bipolar transistors having collector electrodes connected to a supply terminal and having emitter electrodes connected to an output terminal which is coupled to a source of reference potential via an emitter resistor, R_e . A threshold voltage source, having a predetermined output impedance, R_o , is connected to the base of the second one of the transistors, the base of the first of the transistors being coupled to a source of input signal to be limited. A capacitor is coupled between the collector and base electrodes of the second transistor the emitter of which is coupled to a given one of its base and collector electrodes via a further resistor, R_d .

In accordance with a further feature of the invention, the emitter resistor R_e , the further resistor R_d and the output impedance R_o of the threshold voltage source are scaled such that $R_e > R_d$ and $R_d > R_o$.

The foregoing and further features of the invention are shown in the accompanying drawing wherein:

FIGURE 1 is a detailed schematic diagram of a first embodiment of the invention; and

FIGURE 2 is a detailed schematic diagram of a second embodiment of the invention.

The limiter circuit of FIGURE 1 comprises first and second bipolar transistors, Q_1 and Q_2 having collector electrodes connected to a supply terminal 3 for receiving a source of supply

voltage (+Vcc), having emitter electrodes commonly connected at circuit node "A" to an output terminal 2 and coupled to a source of reference potential 4 (ground) via a first resistor Re. A threshold voltage source 5 is connected at circuit node "B" to the base of the second transistor Q2. A capacitor C1 is coupled between the collector and base electrodes of the second transistor Q2 and a second resistor Rd is coupled between the emitter and collector electrodes of the second transistor. In a subsequent embodiment of the invention, the second resistor Rd is connected between the base and collector electrodes of the second transistor.

The threshold signal source 5 (outlined in phantom) comprises a third resistor R1 coupled between the base electrode of the second transistor Q2 and a fourth resistor R2 coupled between the base electrode of the second transistor Q2 and the source of ground potential 4. Resistors R3 and R4, thus connected form a potential divider for developing the threshold voltage Vt for the limiter.

It is desirable for optimum compensation for delay of transistor Q2 that the source resistance for the base of transistor Q2 from the collector supply Vcc be less than the value of resistor Rd which, in turn, is selected to be less than the value of resistor Re. Stated in mathematical terms, $Re > Rd > R1$. A useful approximation is to select the Thevenin equivalent impedance of source 5 to be less than the value of resistor Rd. The equivalent impedance or "output" impedance of source 5 is given by the relationship $R_o = (R1)(R2)/(R1+R2)$. Using this relationship, Ro is selected to be less than Rd which is selected to be less than Re. Desirably, the value of capacitor C1 is selected to be substantially greater than the total capacitance including stray capacitances (not shown) between the base and emitter electrodes of the second transistor Q2.

In the foregoing description, terminals 1 and 2 and transistor Q1 form a first circuit path which provides the function of coupling the input signal IN to the output terminal 2 via the base emitter path of the first transistor Q1. The connections of the output terminal 2, the threshold source 5 and the transistor Q2

form a second circuit path which provides the function of coupling the threshold signal V_t to the output terminal 2 via the base emitter path of the second transistor Q2. The connections of supply terminal 3 and transistors Q1 and Q2 form a third circuit path which provides the function of applying the supply voltage V_{cc} to the collector electrodes of the first and second transistors. The connections of the output terminal 2 and first and second resistors R_e and R_d forms a fourth circuit path that provides the function of coupling the output terminal to the source of reference potential via the first resistor and to a selected one of the base and collector electrodes of the second transistor via the second resistor. In this example, the selected electrode is the collector electrode. Lastly, the connections of capacitor C1 and transistor Q2 forms a fifth circuit path providing the function of coupling the capacitor between the base and collector electrodes of the second transistor. As noted above, it is desirable that the second and fourth circuit path element values are selected to exhibit an impedance inequality in which $R_e > R_d > R_1$ wherein R_e and R_d are the values of the first and second resistors, respectively, and R_1 is the source impedance for the base of transistor Q2 from the supply V_{cc} . A useful approximation is $R_e > R_d > R_o$ wherein R_o is the output impedance of the threshold signal source.

As previously discussed, the main problem in limiting small fast pulses is one of limiter delay. It is herein recognized that in the example of FIGURE 1 the principal source of delay is due mainly to the input capacitance of the second transistor Q2. This transistor has to be charged through the emitter resistor R_e and the threshold source impedance R_1 . Consequently, the feedback voltage applied to the emitter of transistor Q1 is delayed with respect to the input signal voltage I_N by the time to charge the base-emitter capacitance of the transistor Q2 and any stray capacitances associated therewith. If resistor R_d and capacitor C1 were not present in the circuit, this charging delay would cause the input pulse to be cut-off not flat, but slashed. Moreover, in the absence of R_d and C1, in the case of very narrow pulses the cut

never even reaches the predetermined threshold voltage V_t of source 5.

To speed up the response the output impedance of source 5 is bypassed by capacitor C1 and resistor Rd provides current to circuit node "A" which provides what will herein be called "preliminary" clipping. The level of this preliminary clipping is controlled by selecting resistors Rd and Re to produce a voltage at node A at a level a little bit lower than the needed threshold (i.e., less than V_t minus V_{be} of Q2).

Finally, it has been found very desirable in achieving maximum response speed if the resistance values are scaled as previously described to satisfy the inequality $R_e > R_d > R_1$ or, at the least $R_e > R_d > R_o$. Exemplary values are: 15k-Ohms for resistor Re, 9.1 k-Ohms for resistor Rd, and 200 Ohms for R1 and about 1000 pico-Farads for capacitor C1. Other suitable values may, of course, be selected in a specific application to satisfy specific requirements of supply voltage, circuit power dissipation, threshold voltage requirements and so forth. The value of the capacitor C1, desirably, is selected to be substantially greater than the total capacitance between the base and emitter electrodes of the second transistor Q2. The exemplary value noted above is more than an order of magnitude greater than the base emitter capacitance and stray capacitance associated with transistor Q2.

The example of FIGURE 1 may be modified as shown in FIGURE 2 to provide improved precision. In FIGURE 2 the resistor Rd is coupled between the emitter and base electrodes of the second transistor Q2 and the entire circuit has been formed in an integrated circuit 200. Integration provides close matching of transistor threshold voltages and resistor tolerances and values as well as improved reliability.

Other changes may be made in the embodiments herein described. For example, in the discrete version of the limiter of FIGURE 1 the threshold voltage source may be replaced by a potentiometer to facilitate precise adjustment of the threshold voltage V_t . The same change could be done in the

integrated circuit version of FIGURE 2 by making circuit node B available for external connection to a potentiometer and omitting source 5. The potentiometer connections would be across terminals 3 and 4 with the wiper coupled to node B.

- 5 A further change in the disclosed embodiments would be to replace the NPN transistor Q1 and Q2 with PNP transistors. This change (with appropriate changes in the relative supply polarities) will enable fast limiting of positive going pulses whereas use of NPN transistors, as shown, provides fast limiting of
10 negative going pulses.

Claims:

1. A method for limiting an input signal (IN), said method comprising the steps of:
 - 5 coupling said input signal (IN) to an output terminal (2) via the base emitter path of a first transistor (Q1);
 - coupling a threshold signal (V_t) to said output terminal via the base emitter path of a second transistor (Q2);
 - applying a supply voltage ($+V_{cc}$) to the collector
 - 10 electrodes of said first and second transistors;
 - coupling said output terminal (2) to a source of reference potential (4) via a first resistor (R_e) and to a selected one of the base and collector electrodes of the second transistor (Q2) via a second resistor (R_d); and
 - 15 coupling a capacitor (C_1) between the base and collector electrodes of said second transistor (Q2).
2. The method of claim 1 further comprising the steps of:
 - 20 selecting a value for said first resistor (R_e) that is greater than the value of said second resistor (R_d); and
 - selecting an output impedance for said source of limiting signal that is less than the value of said second resistor.
- 25 3. Apparatus for limiting an input signal, said apparatus comprising:
 - a first circuit path for coupling said input signal to an output terminal via the base emitter path of a first transistor;
 - a second circuit path for coupling a threshold signal to
 - 30 the output terminal via the base emitter path of a second transistor;
 - a third circuit path for applying a supply voltage to the collector electrodes of the first and second transistors;
 - a fourth circuit path for coupling the output terminal
 - 35 to a source of reference potential via a first resistor and to a



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selected one of the base and collector electrodes of the second transistor via a second resistor;

a fifth circuit path for coupling a capacitor between the base and collector electrodes of said second transistor.

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4. The apparatus as recited in Claim 3 wherein said second circuit path and said fourth circuit path are selected to exhibit an impedance inequality in which $R_e > R_d > R_o$ wherein R_e and R_d are the values of the first and second resistors, 10 respectively, and R_o is the an output impedance of the threshold signal source.

5. A pulse limiter, comprising:

first (Q1) and second (Q2) bipolar transistors having 15 collector electrodes connected to a supply terminal (3), having emitter electrodes commonly connected to an output terminal (2) and coupled to a source of reference potential (5) via a first resistor (R_e);

a threshold voltage source (5) connected to the base of 20 said second transistor (Q2);

a capacitor (C1) coupled between the collector and base electrodes of said second transistor (Q2); and

a second resistor (R_d) coupled between the base electrode and a selected one of the base and collector electrodes of 25 said second transistor (Q2).

6. The pulse limiter as recited in Claim 5 wherein:

said first resistor (R_e) is of a value greater than that of said second resistor (R_d);

30 said threshold voltage source (5) exhibits a given output impedance; and

said second resistor (R_d) is of a value greater than said given output impedance of said threshold voltage source (5).

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7. The pulse limiter as recited in Claim 5 wherein:
said capacitor (C1) is selected to be substantially
greater in value than the total capacitance, including strays,
between the base and emitter electrodes of said second transistor
5 (Q2).

8. The pulse limiter as recited in Claim 5 wherein said
threshold voltage source (5) comprises:
third (R1) and fourth (R2) resistors coupled between
10 the base electrode of said second transistor (Q2) and respective
ones of said supply terminal (3) and said source of reference
potential (4); and
said third resistor (R1) exhibits a resistance selected
to be less than the value of said second resistor (Rd).

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9. The pulse limiter as recited in any of Claims 5-8
wherein said first (Q1) and second (Q2) transistors, said first (Re)
and second (Rd) resistors, said threshold voltage source (5) and
said capacitor (C1) are formed in an integrated circuit and
20 wherein said second resistor (Rd) is coupled between the base and
emitter electrodes of said second transistor (Q2).

10. The pulse limiter as recited in any of Claims 5-8
wherein said first (Q1) and second transistors (Q2), said first (Re)
25 and second (Rd) resistors, said threshold voltage source (5) and
said capacitor (C1) are formed in an integrated circuit (200) and
wherein said second resistor (Rd) is coupled between the base and
collector electrodes of said second transistor (Q2).

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