

Claims:

1. A microelectronic assembly, comprising:

a redistribution layer (RDL) having a first face and an opposing second face;
a first die at the second face of the RDL, the first die having a first face and an opposing second face, the first face including first conductive contacts having a first pitch and arranged in a first pattern, second conductive contacts having a second pitch and arranged in a second pattern, and third conductive contacts having a third pitch and arranged in a third pattern, wherein the second pitch is different than the first pitch, and wherein the third pitch is different than the first pitch and the second pitch;
a second die, embedded in the RDL between the first face of the RDL and the first face of the first die, having a first face and an opposing second face, wherein the second face of the second die includes second conductive contacts having the second pitch and arranged in the second pattern, and wherein respective ones of the second conductive contacts of the second die are electrically coupled to respective ones of the second conductive contacts of the first die; and
a third die, embedded in the RDL between the first face of the RDL and the first face of the first die, having a first face and an opposing second face, wherein the second face of the third die includes third conductive contacts having the third pitch and arranged in the third pattern, and wherein respective ones of the third conductive contacts of the third die are electrically coupled to respective ones of the third conductive contacts of the first die.

2. The microelectronic assembly of claim 1, wherein the first

face of the first die further includes fourth conductive contacts having the second pitch and arranged in a fourth pattern, wherein the second face of the third die further includes fourth conductive contacts having the second pitch and arranged in the fourth pattern, and wherein respective ones of the fourth contacts of the third die are electrically coupled to respective ones of the fourth conductive contacts of the first die.

3. The microelectronic assembly of claim 1, wherein the first face of the first die further includes fourth conductive contacts having a fourth pitch and arranged in a fourth pattern, wherein the second face of the third die further includes fourth conductive contacts having the fourth pitch and arranged in the fourth pattern, and wherein respective ones of the fourth contacts of the third die are electrically coupled to respective ones of the fourth conductive contacts of the first die.

4. The microelectronic assembly of claim 1, wherein the first face of the first die further includes fourth conductive contacts having a fourth pitch and arranged in a fourth pattern, wherein the fourth pitch is different from the first, second, and third pitches, and the microelectronic assembly further comprises:

a fourth die, embedded in the RDL between the first face of the RDL and the first face of the first die, having a first face and an opposing second face, wherein the second face of the fourth die includes fourth conductive contacts having the fourth pitch and arranged in the fourth pattern, and wherein respective ones of the fourth conductive contacts of the fourth die are electrically coupled to respective ones of the fourth conductive contacts of the first die.

5. The microelectronic assembly of claim 1, wherein the RDL comprises one or more interconnect structures and the second die is between the first surface of the first die and at least a portion of the RDL.

6. The microelectronic assembly of claim 5, wherein at least one of:
one interconnect structure of the RDL includes a conductive pathway between at least one first conductive contact of the first die and at least one conductive contact at the first surface of the RDL;
one interconnect structure of the RDL includes a conductive pathway between at least one second conductive contact of the second die and at least one conductive contact at the first surface of the RDL;
one interconnect structure of the RDL includes a conductive pathway between at least one second conductive contact of the first die and at least one second conductive contact of the second die; and
one interconnect structure of the RDL includes a conductive pathway between at least one second conductive contact of the second die and one third conductive contact of the third die.

7. The microelectronic assembly of claim 1, wherein the second die includes a die substrate, a metallization stack, and a device layer between the die substrate and the metallization stack, and wherein the die substrate is between the package substrate and the device layer.
8. The microelectronic assembly of claim 1, wherein the second die includes a die substrate, a metallization stack, and a device layer between the die substrate and the metallization stack, and wherein the device layer is between the package substrate and the die substrate.
9. The microelectronic assembly of claim 1, wherein the second die includes a first metallization stack, a second metallization stack, and a device layer between the first metallization stack and the second metallization stack.
10. The microelectronic assembly of claim 9, further comprising an insulating layer between the plurality of second dies and the first die.
11. The microelectronic assembly of claim 10, wherein at least two of the plurality of second dies are interconnected via interconnect structures of the insulating layer.
12. The microelectronic assembly of claim 1, wherein the second die is an individual one of a plurality of second dies.
13. The microelectronic assembly of claim 12, wherein at least one second die has a first thickness and at least one other second die has a second thickness that is different than the first thickness of the at least one second die.
14. A computing device, comprising:
 - a composite die, wherein the composite die includes:
 - a redistribution layer (RDL) having a first face and an opposing second face;
 - a first die at the second face of the RDL, the first die having a first face and an opposing second face, the first face including first conductive contacts having a first pitch and arranged in a first pattern, second conductive contacts having a second pitch and arranged in a second pattern, and third conductive contacts having a third pitch and arranged in a third pattern, wherein the second pitch is different than the first pitch, and wherein the third pitch is different than the first pitch and the second pitch; and
 - a second die embedded in the RDL between the first face of the RDL and the first face of the first die,

the second die further including a first face and an opposing second face, wherein the second face of the second die includes second conductive contacts having the second pitch and arranged in the second pattern, and wherein respective ones of the second conductive contacts of the second die are electrically coupled to respective ones of the second conductive contacts of the first die;

a third die, embedded in the RDL between the first face of the RDL and the first face of the first die, having a first face and an opposing second face, wherein the second face of the third die includes third conductive contacts having the third pitch and arranged in the third pattern, and wherein respective ones of the third conductive contacts of the third die are electrically coupled to respective ones of the third conductive contacts of the first die; and

a substrate at the first face of the RDL and electrically coupled to conductive contacts on the first surface of the RDL.

15. The computing device of claim 14, wherein the second die is an individual one of a plurality of second dies.

16. The computing device of claim 15, wherein at least one of:

one second die of the plurality of second dies has a solder interconnection with the first die; and

one second die of the plurality of second dies has a non-solder interconnection with the first die;

17. The computing device of claim 15, wherein at least one second die of the plurality of second dies has a thickness between 10 microns and 30 microns.
18. The computing device of claim 15, wherein at least two second dies of the plurality of second dies are different types of devices.
19. The computing device of claim 15, wherein individual ones of the plurality of second dies have a X-Y area that is smaller than an X-Y area of the first die.