A METHOD TO REDUCE COMPRESSIVE STRESS IN THE SILICON SUBSTRATE DURING SILICIDATION

ABSTRACT

A method for siliciding source/drain junctions is described wherein compressive stress of the underlying silicon is avoided by the insertion of a buffer layer between the silicide and the silicon. A gate electrode and associated source/drain extensions are provided in and on a semiconductor substrate. A buffer oxide layer is deposited overlying the semiconductor substrate and the gate electrode. A polysilicon layer is deposited overlying the buffer oxide layer. The polysilicon layer will form the source/drain junctions and silicon source. The source/drain junctions are silicided whereby the buffer oxide layer provides compressive stress relief during the siliciding.

Figure 11