CLAIMS

1. A semiconductor memory device comprising:

a first bit line;

a first capacitor; and

a first select transistor and a first memory cell transistor that are coupled in series between the first bit line and the first capacitor;

a second capacitor;

a second select transistor and a second memory cell transistor that are coupled in series between the first bit line and the second capacitor;

a first select gate line coupled to a gate of the first select transistor;

a second select gate line coupled to a gate of the second select transistor; and

a first word line coupled to a gate of the first memory transistor and a gate of the second memory transistor.

2. The semiconductor memory device according to claim 1, further comprising a third memory transistor, wherein

the first memory cell transistor and the third memory cell transistor being coupled in series between the first select transistor and the first capacitor.

3. The semiconductor memory device according to claim 1, wherein the first capacitor includes a first end configured to be electrically coupled to the first bit line, and a second end in a floating state.

4. The semiconductor memory device according to claim 1, wherein the first capacitor includes a first end configured to be electrically coupled to the first bit line, and a second end that is grounded.

5. The semiconductor memory device according to claim 1, comprising a first memory string and a second memory string, wherein

the first memory string includes the first capacitor, the first select transistor, and the first memory transistor,

the second memory string includes the second capacitor, the second select transistor, and the second memory transistor, and

the first memory string and the second memory string are electrically coupled to the first bit line.

6. The semiconductor memory device according to claim 1, comprising:

a second bit line different from the first bit line;

a first memory string being electrically coupled to the first bit line; and

a second memory string being electrically coupled to the second bit line, wherein

the first memory string includes the first capacitor, the first select transistor, and the first memory transistor,

the second memory string includes a third capacitor, a third select transistor, and a fourth memory transistor,

the third select transistor and the fourth memory transistor are coupled in series between the second bit line and the third capacitor.