

Claims

What is claimed:

1. A method of ~~manufacturing~~ making a semiconductor device, comprising:
 - providing a ~~temporary carrier~~ semiconductor die;
 - ~~mounting a~~ depositing an encapsulant over the semiconductor die ~~over the temporary carrier with an active surface oriented toward the temporary carrier~~;
 - forming a first interconnect structure over the semiconductor die and the encapsulant;
 - ~~depositing an~~ forming a second interconnect structure over the encapsulant ~~over the temporary carrier and semiconductor die~~ and the semiconductor die opposite the first interconnect structure;
 - ~~removing the temporary carrier~~;
 - ~~forming a first interconnect structure over the active surface and encapsulant~~;
 - ~~forming a second interconnect structure over the encapsulant and a back surface of the semiconductor die opposite the active surface~~;
 - ~~forming a plurality of vias through the second interconnect structure, encapsulant, and first interconnect structure~~;
 - ~~forming a first conductive layer in the vias to electrically connect the first interconnect structure and second interconnect structure~~; and
 - ~~forming a first insulating layer over the first interconnect structure and second interconnect structure~~.
 - forming a first protective layer over the second interconnect structure;

forming a via through the first protective layer, first interconnect structure, the second interconnect structure, and the encapsulant around the semiconductor die;

removing the first protective layer;

forming a first conductive layer in the via and extending over the first and second interconnect structures to electrically connect the first interconnect structure and second interconnect structure; and

forming a first insulating layer over the first interconnect structure and first conductive layer.

2. The method of claim 1, further including~~+~~

~~forming a first protective layer over the first interconnect structure prior to forming the vias; and~~

~~—forming~~ providing a second protective layer over the ~~second~~first interconnect structure prior to forming the vias~~s~~.

3. The method of claim 1, wherein forming the first interconnect structure includes:

forming a second insulating layer over the semiconductor die active surface and encapsulant; and

forming a second conductive layer over the second insulating layer ~~with electroless plating and electrolytic plating;~~

~~—forming a third insulating layer over the second insulating layer and second conductive layer; and~~

~~—forming a third conductive layer over the third insulating layer and second conductive layer.~~

4. The method of claim 1, wherein forming the second interconnect structure includes:

forming a second insulating layer over the encapsulant and ~~back surface of the~~ semiconductor die; and

forming a second conductive layer over the second insulating layer ~~with electroless plating and electrolytic plating;~~

~~—forming a third insulating layer over the second insulating layer and second conductive layer; and~~

~~—forming a third conductive layer over the third insulating layer and second conductive layer.~~

5. The method of claim 1, further including forming the first insulating layer in the vias.

6. The method of claim 1, further including ~~mounting~~ disposing a discrete semiconductor component over the first interconnect structure.

7. The method of claim 1, further including forming a second conductive layer over the ~~active surface prior to mounting the semiconductor die over the temporary carrier.~~

8. The method of claim 1, further including removing a portion of the encapsulant and semiconductor die.

~~89.~~ A method of ~~manufacturing~~ making a semiconductor device, comprising:

providing a ~~carrier;~~

~~— mounting a semiconductor die over the carrier;~~

depositing an encapsulant over the ~~carrier and~~ semiconductor die;

~~removing the carrier;~~

forming a first interconnect structure over the encapsulant and a first surface of the semiconductor die;

forming a second interconnect structure over the encapsulant and a second surface of the semiconductor die opposite the first surface of the semiconductor die;

~~forming a plurality of vias through the second interconnect structure, encapsulant, and first interconnect structure; —~~

forming a first ~~conductive~~ protective layer ~~in the vias to electrically connect over~~ the first interconnect structure ~~and second interconnect structure; and~~

~~forming a first insulating layer over the first interconnect structure and second interconnect structure~~

forming a via through the first protective layer, first interconnect structure, second interconnect structure, and encapsulant;

removing the first protective layer; and

forming a first conductive layer in the via to electrically

connect the first interconnect structure and second interconnect structure.

~~9. The method of claim 8, further including forming a protective layer over the first interconnect structure prior to forming the vias.~~

~~10. The method of claim 8, further including forming a protective layer over the second interconnect structure prior to forming the vias.~~

~~11. The method of claim 8, further including removing a portion of the encapsulant and second surface of the semiconductor die.~~

~~12. The method of claim 8, wherein forming the first interconnect structure includes:~~

~~—— forming a second insulating layer over the first surface and encapsulant;~~

~~—— forming a second conductive layer over the second insulating layer with electroless plating and electrolytic plating;~~

~~—— forming a third insulating layer over the second insulating layer and second conductive layer; and~~

~~—— forming a third conductive layer over the third insulating layer and second conductive layer.~~

~~13. The method of claim 8, wherein forming the second interconnect structure includes:~~

~~—— forming a second insulating layer over the encapsulant and second surface of the semiconductor die;~~

~~—— forming a second conductive layer over the second insulating layer with electroless plating and electrolytic plating;~~

~~—— forming a third insulating layer over the second insulating layer and second conductive layer; and~~

~~—— forming a third conductive layer over the third insulating layer and second conductive layer.~~

~~14. The method of claim 8, further including forming the first insulating layer in the vias.~~

~~15. A method of manufacturing a semiconductor device, comprising:~~

- ~~— providing a carrier;~~
- ~~— mounting a semiconductor die over the carrier;~~
- ~~— depositing an encapsulant over the carrier and semiconductor die;~~
- ~~— removing the carrier;~~
- ~~— forming a first interconnect structure over the encapsulant and a first surface of the semiconductor die;~~
- ~~— forming a plurality of vias through the first interconnect structure and partially through the encapsulant to a position above a second surface of the semiconductor die opposite the first surface of the semiconductor die;~~
- ~~— removing a portion of the encapsulant over the second surface of the semiconductor die to open the vias;~~
- ~~— forming a first conductive layer in the vias;~~
- ~~— forming a second interconnect structure over the encapsulant and second surface of the semiconductor die; and~~
- ~~— forming a first insulating layer over the first interconnect structure and second interconnect structure.~~

~~16. The method of claim 15, wherein forming the first interconnect structure includes:~~

- ~~— forming a second insulating layer over the first surface and encapsulant;~~
- ~~— forming a second conductive layer over the second insulating layer with electroless plating and electrolytic plating;~~
- ~~— forming a third insulating layer over the second insulating layer and second conductive layer; and~~
- ~~— forming a third conductive layer over the third insulating~~

~~layer and second conductive layer.~~

~~17. The method of claim 15, wherein forming the second interconnect structure includes:~~

~~—— forming a second insulating layer over the encapsulant and second surface of the semiconductor die;~~

~~—— forming a second conductive layer over the second insulating layer with electroless plating and electrolytic plating;~~

~~—— forming a third insulating layer over the second insulating layer and second conductive layer; and~~

~~—— forming a third conductive layer over the third insulating layer and second conductive layer.~~

~~18. The method of claim 15, further including forming the first insulating layer in the vias.~~

~~19. The method of claim 15, further including mounting a discrete semiconductor component over the first interconnect structure.~~

~~20. A semiconductor device, comprising:~~

~~—— a semiconductor die;~~

~~—— an encapsulant deposited over the semiconductor die;~~

~~—— a first interconnect structure formed over the encapsulant and a first surface of the semiconductor die;~~

~~—— a second interconnect structure formed over the encapsulant and a second surface of the semiconductor die opposite the first surface of the semiconductor die;~~

~~—— a plurality of conductive vias formed through the second interconnect structure, encapsulant, and first interconnect~~

~~structure to electrically connect the first interconnect structure and second interconnect structure; and~~
~~— a first insulating layer formed over the first interconnect structure and second interconnect structure.~~

~~21. The semiconductor device of claim 20, wherein a portion of the encapsulant and second surface of the semiconductor die is removed.~~

~~22. The semiconductor device of claim 20, wherein the first interconnect structure includes:~~
~~— a second insulating layer formed over the first surface and encapsulant;~~
~~— a first conductive layer formed over the second insulating layer with electroless plating and electrolytic plating;~~
~~— a third insulating layer formed over the second insulating layer and first conductive layer; and~~
~~— a second conductive layer formed over the third insulating layer and first conductive layer.~~

~~23. The semiconductor device of claim 20, wherein the second interconnect structure includes:~~
~~— a second insulating layer formed over the encapsulant and second surface of the semiconductor die;~~
~~— a first conductive layer formed over the second insulating layer with electroless plating and electrolytic plating;~~
~~— a third insulating layer formed over the second insulating layer and first conductive layer; and~~
~~— a second conductive layer formed over the third insulating layer and first conductive layer.~~

~~24. The semiconductor device of claim 20, wherein the first insulating layer is formed in the vias.~~

~~25. The semiconductor device of claim 20, further including a discrete semiconductor component mounted over the first interconnect structure.~~

10. The method of claim 9, further including forming a second protective layer over the second interconnect structure prior to forming the via.

11. The method of claim 9, wherein forming the first interconnect structure further includes:

forming a second insulating layer over the first surface and encapsulant;

forming a second conductive layer over the second insulating layer with electroless plating and electrolytic plating;

forming a third insulating layer over the second insulating layer and second conductive layer; and

forming a third conductive layer over the third insulating layer and second conductive layer.

12. The method of claim 9, wherein forming the second interconnect structure further includes:

forming a second insulating layer over the encapsulant and second surface of the semiconductor die;

forming a second conductive layer over the second insulating layer with electroless plating and electrolytic plating;

forming a third insulating layer over the second insulating layer and second conductive layer; and

forming a third conductive layer over the third insulating layer and second conductive layer.

13. The method of claim 9, further including forming the first insulating layer in the via.

14. A method of making a semiconductor device, comprising:

providing a semiconductor die;

depositing an encapsulant over the semiconductor die;

forming a first interconnect structure over the encapsulant and the semiconductor die;

forming a second interconnect structure over the encapsulant and the semiconductor die opposite the first interconnect structure;

forming a first protective layer over the second interconnect structure;

forming a via through the first interconnect structure, second interconnect structure, encapsulant, and first protective layer;

removing an entirety of the first protective layer;
and

forming a first conductive layer in the via to electrically connect the first interconnect structure and second interconnect structure.

15. The method of claim 14, further including providing a second protective layer over the first interconnect structure prior to forming the via.

16. The method of claim 14, wherein forming the first interconnect structure includes:

forming an insulating layer over the encapsulant and semiconductor die; and

forming a second conductive layer over the insulating layer.

17. The method of claim 14, wherein forming the second interconnect structure includes:

forming an insulating layer over the encapsulant and semiconductor die; and

forming a second conductive layer over the insulating layer.

18. The method of claim 14, further including removing a portion of the encapsulant and semiconductor die.

19. The method of claim 14, further including forming an insulating layer in the via.

20. The method of claim 14, further including disposing a discrete semiconductor component over the first interconnect structure.

21. A method of making a semiconductor device, comprising:

providing a semiconductor die;

depositing an encapsulant over the semiconductor die;

forming a first interconnect structure over the encapsulant and semiconductor die;

providing a first protective layer over the first interconnect structure;

forming a second interconnect structure over the encapsulant and semiconductor die opposite the first

interconnect structure;

forming a second protective layer over the second
interconnect structure;

forming a via through the second protective layer, first
interconnect structure, encapsulant, second interconnect
structure and into the first protective layer;

removing an entirety of the first protective layer;

removing an entirety of the second protective layer; and

forming a conductive layer in the via and extending over
the first and second interconnect structures to electrically
connect the first and second interconnect structures.

22. The method of claim 21, wherein forming the first
interconnect structure includes:

forming an insulating layer over the semiconductor die; and

forming a first conductive layer over the insulating layer.

23. The method of claim 21, wherein forming the second
interconnect structure includes:

forming an insulating layer over the semiconductor die; and

forming a first conductive layer over the insulating layer.

24. The method of claim 21, further including forming an
insulating layer in the via.

25. The method of claim 21, further including disposing a
discrete semiconductor component over the first interconnect
structure.

26. The method of claim 21, further including removing a
portion of the encapsulant and semiconductor die.