METHOD OF FORMING DOUBLE-GATED SILICON-ON-INSULATOR (SOI) TRANSISTORS WITH REDUCED GATE TO SOURCE-DRAIN OVERLAP CAPACITANCE

ABSTRACT

A method of forming a double-gated transistor comprising the following sequential steps. A substrate having an SOI structure formed thereover is provided. The SOI structure including a lower SOI oxide layer and an upper SOI silicon layer. The SOI silicon layer is patterned to form a patterned SOI silicon layer including a source region and a drain region connected by a channel portion. An encasing oxide layer is formed over the patterned SOI silicon layer to form an encased patterned SOI silicon layer. A patterned dummy layer is formed over the encased patterned SOI silicon layer. The patterned dummy layer having an opening, with exposed side walls, exposing: the channel portion of the encased patterned SOI silicon layer; and portions of the upper surface of the SOI oxide layer. Offset spacers are over the exposed side walls of the patterned dummy layer opening. The SOI oxide layer is etched while minimizing the undercut portions of the upper surface of the SOI oxide layer are undercut into the SOI oxide layer to form a minimal undercut. The minimizing undercutting process also removing the offset spacers and the encasing oxide layer over the channel portion of the patterned SOI silicon layer. A conformal oxide layer is

formed around the channel portion of the patterned SOI silicon layer. A gate is formed within the patterned dummy layer opening. The gate including an upper gate above the patterned SOI silicon layer and a lower gate under the patterned SOI silicon layer. The patterned dummy layer is then removed to form the double-gated transistor.

Figure 10