CLAIMS

1. A signal line structure, comprising:

a plurality of parallel signal lines, wherein each of the signal lines is maintained in a drive state at any time;

wherein two ends of each of the signal lines are respectively connected to a first driver and a second driver, and at the same time, only one of the first driver and the second driver of the same signal line is maintained in a drive state;

wherein the first driver is maintained in the drive state when a first enable signal is at a first level and maintained in a high-impedance state when the first enable signal is at a second level; and the second driver is maintained in the drive state when a second enable signal is at the first level and maintained in the high-impedance state when the second enable signal is at the second level;

wherein the second enable signal is obtained by inverting the first enable signal through an inverter.

2. The signal line structure according to claim 1, wherein the first level is a high level, and the second level is a low level.

3. The signal line structure according to any one of claims 1, wherein the first driver or the second driver comprises at least one gating inverter, and the gating inverter is provided with an input terminal electrically connected to an input signal, an enable terminal connected to the first enable signal or the second enable signal, and an output terminal electrically connected to the signal line.

4. The signal line structure according to claim 1, wherein the plurality of parallel signal lines comprise odd data lines and even data lines arranged in a staggered manner, the odd data lines are configured to transmit odd signals obtained according to sampling of odd clocks, the even data lines are configured to transmit even signals obtained according to sampling of even clocks, and there is a phase difference of 180 degrees between the odd clock and the even clock; and the first enable signal

corresponding to the odd data lines and the first enable signal corresponding to the even data lines have different phases, and the second enable signal corresponding to the odd data lines and the second enable signal corresponding to the even data lines have different phases.

5. The signal line structure according to claim 4, wherein there is a phase difference of 180 degrees between the first enable signal corresponding to the odd data lines and the first enable signal corresponding to the even data lines, and there is a phase difference of 180 degrees between the second enable signal corresponding to the odd data lines and the second enable signal corresponding to the even data lines.

6. A signal line driving method, applied to the signal line structure according to any one of claims 1-5, wherein the signal line driving method comprises:

controlling a plurality of parallel signal lines to be maintained in a drive state at any time;

wherein two ends of each of the signal lines are respectively provided with a first driver and a second driver; and controlling the parallel signal lines to be maintained in the drive state at any time comprises:

controlling, at the same time, only one of the first driver and the second driver of the same signal line to be maintained in a drive state;

wherein the first driver or the second driver comprises at least one gating inverter, and the gating inverter is provided with an input terminal electrically connected to an input signal, an enable terminal connected to a first enable signal or a second enable signal, and an output terminal electrically connected to the signal line; and the controlling, at the same time, only one of the first driver and the second driver of the same signal line to be maintained in the drive state comprises:

inputting the first enable signal at a first level into an enable terminal of the first driver so as to enable the first driver to be maintained in the drive state, and, at the same time, inputting the second enable signal at a second level into an enable terminal of the second driver so as to enable the second driver to be maintained in a

high-impedance state; or inputting the first enable signal at the second level into the enable terminal of the first driver so as to enable the first driver to be maintained in the high-impedance state, and, at the same time, inputting the second enable signal at the first level into the enable terminal of the second driver so as to enable the second driver to be maintained in the drive state.

7. The signal line driving method according to claim 6, wherein the first driver is provided with an input terminal for receiving a first input signal, an enable terminal connected to a first node, and an output terminal connected to the signal line; the second driver is provided with an input terminal for receiving a second input signal, an enable terminal connected to a second node, and an output terminal connected to the signal line; the first node is configured to receive a driver enable signal; the second node and the first node are connected through an odd number of inverters; and controlling, at the same time, only one of the first driver and the second driver to be maintained in the drive state comprises:

in response to a first input signal arrival message, setting the driver enable signal to be at a first level, such that the first driver is maintained in the drive state, and the second driver is maintained in a high-impedance state; and

in response to a second input signal arrival message, setting the driver enable signal to be at a second level, such that the second driver is maintained in the drive state, and the first driver is maintained in the high-impedance state.

8. The signal line driving method according to claim 6, wherein the first level is a high level, and the second level is a low level.

9. The signal line driving method according to claim 6, wherein two ends of each of the signal lines are respectively provided with a first driver and a second driver; the plurality of signal lines comprise odd data lines and even data lines; controlling the parallel signal lines to be maintained in the drive state at any time comprises:

for a same odd data line, inputting a first enable signal at a first level into the first

driver, and inputting a second enable signal at a second level into the second driver so as to enable the odd data line to be maintained in the drive state; or for the same odd data line, inputting the first enable signal at the second level into the first driver, and inputting the second enable signal at the first level into the second driver so as to enable the odd data line to be maintained in the drive state; and

for a same even data line, inputting the first enable signal at the first level into the first driver, and inputting the second enable signal at the second level into the second driver so as to enable the even data line to be maintained in the drive state; or for the same even data line, inputting the first enable signal at the second level into the first driver, and inputting the second enable signal at the first level into the second driver so as to enable the even data line to be maintained in the drive state; wherein

the first enable signal corresponding to the odd data lines and the first enable signal corresponding to the even data lines have different phases, and the second enable signal corresponding to the odd data lines and the second enable signal corresponding to the even data lines have different phases.