ABSTRACT

In some embodiments, a non-volatile memory device includes a first semiconductor layer that includes a first memory cell array disposed on a first cell region, a second memory cell array disposed on a second cell region, and a first metal pad. The non-volatile memory device further includes a second semiconductor layer that includes a first peripheral circuit disposed on a first region and coupled to the first memory cell array, a second peripheral circuit disposed on a second region and coupled to the second memory cell array, and a second metal pad. The first region includes a first peripheral circuit region that overlaps the first cell region in the vertical direction, and a second peripheral circuit region that does not overlap the first cell region in the vertical direction, and the second region overlaps the second cell region in the vertical direction.

FIG. 6